SOLAR MOBILE PHONE BATTERY CHARGER USING PHOTOVOLTAIC CELL

[1] OLUWALEKE AFOLABI ABIMBOLA, [2] ESAN EMMANUEL ADEYEMI, [3]OJO TEMIDAYO ABOLADE

[1] Department of Electrical and Electronics Engineering, Olabisi Onabanjo University, Ago-Iwoye, Ogun State, Nigeria.
[2] Department of Electrical and Electronics Engineering, University of Ibadan, Ibadan, Oyo State, Nigeria.
[3] Department of Physics and Electronics Technology, University of Benin, Benin, Edo State, Nigeria.

ABSTRACT

Solar energy is the light and radiant heat from the Sun that influences Earth's climate and weather and sustains life. Solar power is sometimes used as a synonym for solar energy or more specifically to refer to electricity generated from solar radiation. Since ancient times solar energy has been harnessed for human use through a range of technologies. Solar radiation along with secondary solar resources such as wind and wave power,hydroelectricity and biomass account for most of the available flow of renewable energy on Earth. Solar energy technologies can provide electrical generation by heat engine or photovoltaic means, space heating and cooling in active and passive solar buildings; potable water via distillation and disinfection, day-lighting, hot water, thermal energy for cooking, and high temperature process heat for industrial purposes. Another milestone in solar technology is the charging of mobile phone batteries , using solar panels, this has provided a great alternative to the conventional means of electricity generation via generators and so on, much more as telecommunication and information and communication technology has taken over the day to day business activities of human beings across the whole world. Millions of people across the world access internet services via their mobile phones all day long for one transaction or the other, thereby need a more readily available source of energy to recharge their cell phone batteries. Hence, harnessing solar power in this age is of a great benefit, as we all know that power is an integral part of communication, as it is very essential to communicate with one another, equally, it is vital to research into other alternative source of electric power like solar power to sustain our thriving information and communication technology industry.

***KEYWORDS**: Solar energy, Solar radiation, Photovoltaic cell, Heat engine, Hydroelectricity, Solar power, telecommunication, information and communication technology, mobile phone.*

1. INTRODUCTION

This paper involves the design and analysis of a solar mobile phone charger and uses photovoltaic solar cell. Fig 1.1 below shows the generalized block diagram:

1.1 GENERALIZED BLOCK DIAGRAM.

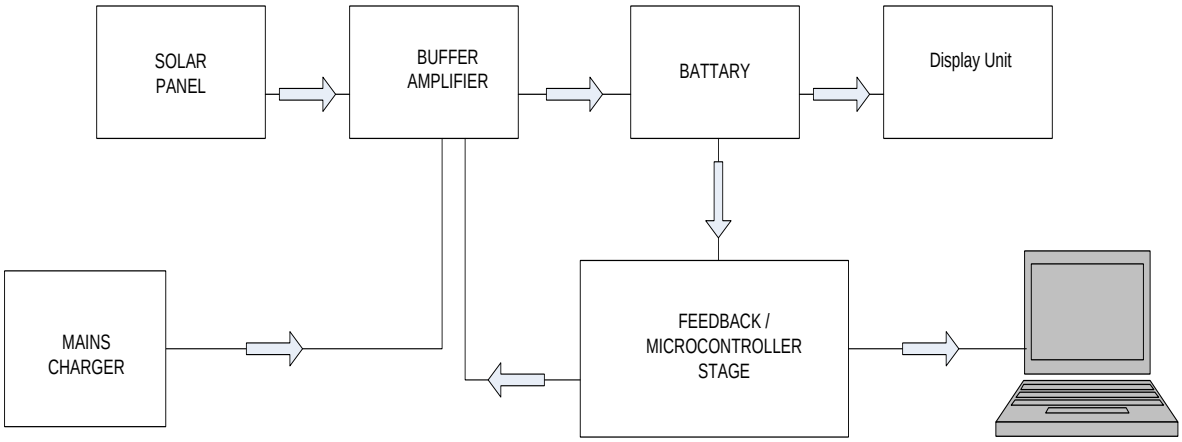


FIG 1.1 Generalized Block Diagram

1.2 DESIGN SPECIFICATIONS:

CHARGING VOLTAGE: 15VDC

CHARGING CURRENT : 5A (maximum).

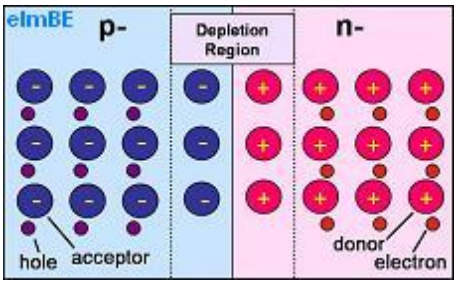
INPUT (MAINS): 220VAC

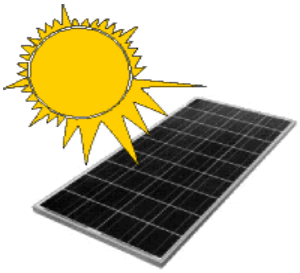
SOLAR PANEL: 12V (60W)

1.3 THEORY OF DEVICES:

1.31 PHOTOVOLTAIC SOLAR PANELS

PV (photovoltaic) Solar Panels generate electricity by the Photovoltaic Effect. Discovered in 1839 by 19yr old Edmund Becquerel, the photovoltaic effect is the phenomenon that certain materials produce electric current when they are exposed to light. For traditional PV solar panels a semiconductor PN junction is manufactured in which two halves of one pure silicon crystal are *doped* with two different dopants (e.g. arsenic, gallium, aluminum, phosphorus). One half of the crystal is left electron deficient (the p-type layer), and one half is left with an excess of electrons (the n-type layer). The dopants in the semiconductor lead to an electric field across the junction between the two halves of the crystal with electrons able to travel in one direction only - from the electron rich half to the electron poor half.





Where the two halves of the crystal meet, there is a depletion region, so called because it is depleted of charge carriers (electrons and holes). Electrons move from the n-type (negative) side to the p-type (positive) side of the crystal recombining with holes. Likewise holes move from the p-type side to the n-type side. As the silicon atoms themselves do not move, any holes which remain uncovered by electrons in the n-type side are left positively charged, and any electrons without holes to cover in the p-type side remain negatively charged. This leaves positive material close to the junction in the n-type side, and negative material close to the junction in the p-type side with a potential between the two sides of around 0.6-0.7 volts in a silicon pn junction. This potential barrier between the p and n-type sides of the crystal prevents further electrons and holes from travelling across the junction until sunlight hits the solar cell and releases electrons with enough energy to overcome the barrier. The light from the sun is made up of packets of energy called *Photons*. Each photon carries an amount of energy corresponding to its wavelength of light. When a photon strikes a solar cell it can do one of three things: pass straight through, be reflected, or be absorbed. If the photon is absorbed, its energy is absorbed by an electron in an atom of the solar cell enabling it to escape from its normal position, cross the junction and fill a hole. The electrons then flow through a load (e.g. charging a battery, lighting a light, or powering a motor), and complete the circuit by recombining with the holes they left behind. In so doing energy from the sunlight has been extracted and used at an efficiency of around 5-15%. This process can be repeated over and over again over the decades of lifetime of solar cells.

1.32 IC TIMERS

The emanation of IC timers eliminated a wide range of mechanical and electromechanical timing devices .It also helped in the generation of clock and oscillator circuits.

Timing circuits are those, which will provide an output change after a predetermined time interval. This is, of course, the action of the monostable multivibrator, which will give time delay from a fraction of a second to several minutes quite accurately.

The most popular of the present IC is the 555 timer, which is available in an eight pin dual-in -line package in both bipolar and CMOS form. The 555 timer is a relatively stable IC capable of being operated as an accurate bi-stable, monostable or astable multivibrators.

The 555 timer is one of the most popular and versatile integrated circuits ever produced. It includes 23 transistors, 2 diodes and 16 resistors on a silicon chip installed in an 8-pin mini dual-in-line package (DIP-8).

The 556 is a 14-pin DIP that combines two 555s on a single chip. The 558 is a 16-pin DIP that combines four slightly modified 555s on a single chip (DIS & THR are connected internally; TR is falling edge sensitive instead of level sensitive). Also available are ultra-low power versions of the 555 such as the 7555 and TLC555. The 7555 requires slightly different wiring using fewer external components and less power.

The 555 has three operating modes:

- Monostable mode: in this mode, the 555 functions as a "one-shot". Applications include timers, missing pulse detection, bounce-free switches, touch switches, Frequency Divider, Capacitance Measurement, Pulse Width Modulation (PWM) etc
- Astable - Free Running mode: the 555 can operate as an oscillator. Uses include LED and lamp flashers, pulse generation, logic clocks, tone generation, security alarms, pulse position modulation, etc.
- Bistable mode or Schmitt trigger: the 555 can operate as a flip-flop, if the DIS pin is not connected and no capacitor is used. Uses include bounce-free latched switches, etc.

Using simply a capacitor and a resistor, the timing interval, i.e. the time during which the output stays low, can be adjusted to the need of the specific application. Thus, the 555 operates in monostable mode.
The interval time *t* is given by

$$t = 1.1 \cdot RC$$

this is the time it takes to charge C to 63% of the applied voltage.

When in astable mode, a resistor (call it R1) is connected between Vcc and the discharge pin (pin 7) and another (R2) is connected between the discharge pin (pin 7) and the trigger (pin 2) and threshold (pin 6) pins that share a common node. Hence the capacitor is charged through R1 and R2, and discharged only through R2, since pin 7 has low impedance to ground during output low intervals of the cycle, therefore discharging the capacitor. The use of R2 is mandatory, since without it the high current spikes from the capacitor may damage the internal discharge transistor.

In the astable mode, the high time from each pulse is given by

$$high = 0.693 \cdot (R1 + R2) \cdot C$$

and the low time from each pulse is given by

$$low = 0.693 \cdot R2 \cdot C$$

where , R1 and R2 are the values of the resistors in ohms and C is the value of the capacitor in farads.

It has a voltage varying gate. The gate is open when the output voltage is low, and the gate is closed when output voltage is high.

The internal circuitry is shown in fig 2.1a below, while fig 2.1b shows the 555 timer DIL package.

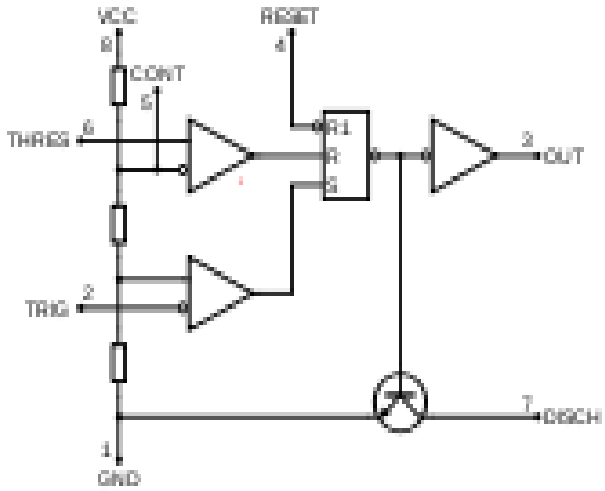


Fig 2.1a 555- Timer Internal Circuitry

Fig 2.1b 555- Timer DIL Package.

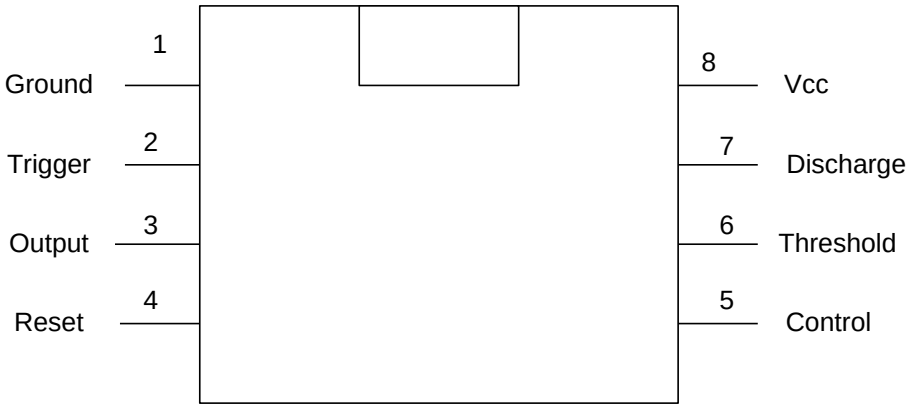


Fig 2.1c 555 timer pin orientations

The functional diagram consists of two comparators, a flip-flop, two control transistors and a high current output stage. The two comparators are actually operational amplifiers that compare input voltage to internal reference voltages which are generated by internal voltage divider of three 5K resistors.

The reference voltage provided is one third and two third of Vcc. When the input voltage to either of the comparators is higher than the reference voltage for the comparator, the amplifier goes to saturation and produces an output signal to trigger the flip-flop. The output of the flip-flop controls the output stage of the timer. The 555 timer chip works from a d. c. supply between 3-15V and can source or sink up to 200mA at its output.

The operation of the 555 timer is better understood by further defining the functions of all the pins. The details regarding connection to be made to pins are as follows.

Pin 1: This is the ground pin and should be connected to the negative side of the supply voltage.

Pin 2: This is the trigger input. A negative going voltage pulse applied to this pin when falling below 1/3Vcc causes the comparator output to change state. The output level then switches from LOW to HIGH. The trigger pulse must be of shorter duration than the time interval set by the external CR network otherwise the output remains high until trigger input is driven high again.

Pin 3: This is the output pin and is capable of sinking or sourcing a load requiring up to 200mV and can drive TTL circuits. The output voltage available is approximately Vcc –1.7V.

Pin 4: This is the reset pin and is used to reset the flip-flop that controls the state of output pin 3. Reset is activated with a voltage level of between 0V and 0.4V and forces the output low regardless of the state of the other flip-flop inputs. If reset is not required, then pin 4 should be connected to same point as pin 8 to prevent accidental resetting.

Pin 5: This is the control voltage input. A voltage applied to this pin allows the timing variations independently of the external timing network. Control voltage may be varied from between 45 to 90 of the Vcc value in monostable mode. In astable mode the variation is from

1.7 to the full value of supply voltage. This pin is connected to the internal voltage divider so that the voltage measurement from here to ground should read 2/3 of the voltage applied to pin 8. If this pin is not used it should be bypassed to ground, typically use a 10nF capacitor. This helps to maintain immunity from noise. The CMOS ICs for most applications will not require the controlled voltage to be decoupled and it should be left unconnected.

Pin 6: This is the threshold input. It resets the flip-flop and hence drives the output low if the applied voltage rises above two-third of the voltage applied to pin 8. Additionally a current of minimum value 0.1 A must be supplied to this pin since this determines the maximum value of resistance that can be connected between the positive side of the supply and this pin. For a 15V supply the maximum value of resistance is 20M.

Pin 7: This is the discharge pin .It is connected to the collector of an npn transistor while the emitter is grounded. Thus when the transistor is turned on, pin 7 is effectively grounded.. Usually the external timing capacitor is connected between pin 7 and ground and is thus discharged when the transistor goes on.

Pin 8: This is the power supply pin and is connected to the positive of the supply. The voltage applied may vary from 4.5V to 16V although devices, which operate up to 18V, are available.

1.33 OTHER PASSIVE COMPONENTS

Passive components are components, which cannot amplify power and require an external power source to operate. They include resistors, capacitors, indicators, and transformers etc. their application range from potential dividers to control of current (as in resistors), filtration of ripples voltages and blocking of unwanted D.C voltages (as in capacitors). They form the elements of the network circuit oscillator stages (LC and RC networks), biasing of transistor circuits and are also used generally for signal conditioning in circuits. Their schematic diagrams and symbols are shown in fig 2.5a-d below.

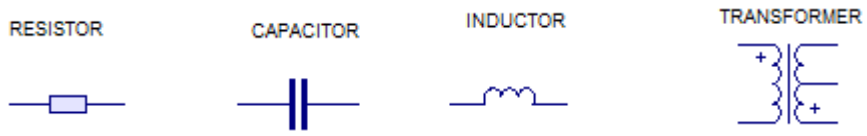


Fig 2.6a-d schematic representation for passive components.

2. METHOD: DESIGN

2.1 PRINCIPLE OF OPERATION.

The solar panel is a 5W solar panel with a voltage output of 7 -12V (depending on the intensity of the sunlight). This output voltage is regulated to give the required charging voltage and current for a mobile phone. The circuit is designed to charge from solar when

there is sunlight and directly from mains voltage at night. Diode polarity protection circuits, ensure that there is no reverse current from the battery when the system is not charging, or when there is no sunlight. The inbuilt charger control inside the mobile phone indicates when battery is fully charged.

If both the solar and mains are connected, charging current will be drained from where there is higher potential difference (mains regulated supply in this case) , while the solar output voltage is ignored.

To charge mobile phones from battery, some certain criteria in terms of charging current and charging voltage must be met in order not to damage the battery. All these are discussed in unit 2.1.

2.2 POWER SUPPLY/ CHARGER STAGE

Charging Requirements for Mobile phones.

Ideally you should not charge a battery with more than 10% of its capacity as current - for example, charge a 2,000mah capacity battery with a current of 200ma or lower. This is particularly important when the batteries are nearing full charge and far less important when they are fully discharged. If you break the 10% rule then overcharging can occur damaging the battery potentially beyond repair and generating heat.

Mobile phone batteries range from (700mA to 2700mA). Designing for worst case, we'll be looking at a charging current of 270mA maximum.

The voltage of the battery is usually 3.6V, hence a charging voltage from 5-6V would suffice.

. The mains charger stage is basically a linear power supply type and involves is step down transformer, Rectifier, Filter capacitor, and voltage regulators (to give a stabilized DC voltage of 5V).

The charger circuit is shown in fig 2.2a below.

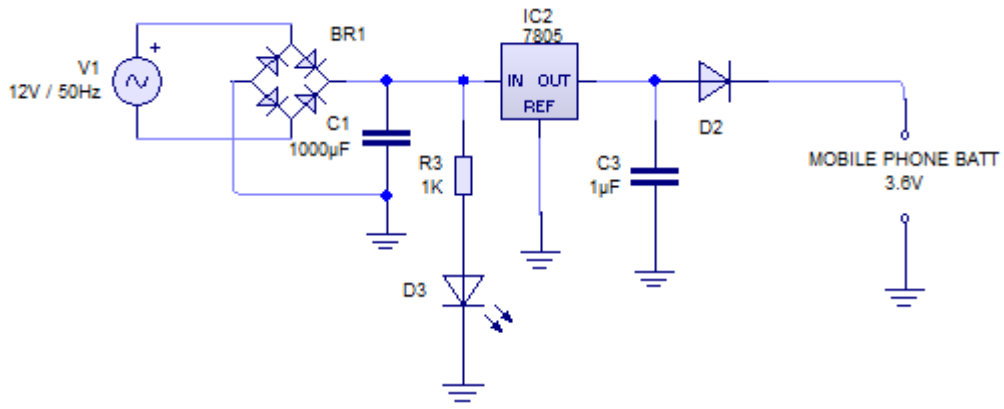


Fig 2.2a Mains Charger Stage.

3. RESULT

3.1 ANALYSIS

We need to get the value of C1 that gives a maximum output current of 300mA at a certain allowable ripple voltage.

$$\frac{dv}{dt} = \frac{1}{c} i \; - - - - - - - - - - - - - (1)$$

Where: dv = ripple voltage

dt = period

c = capacitance value (C1) and,

i = load current

If we set an allowable ripple of 20%, then

$\delta v = 0.2 \; X \; 16.9 = 3.38 \, V \; - - - (16.9V \; being \; the \; peak \; voltage \; \; for \; an \; r.m.s \; of \; 12V \;)$.

From (1), $\quad c = i \frac{dt}{dv} - - - - - - - - - - - - - - - - - - (2)$

$$C = 0.3 \; X \; {}^{0.01}\!/_{3.38} \; - - - - - (for \; i = 0.3A(\max), \; and \; \delta t = 10ms \;)$$
$$= 887.5 \mu F$$
$$= 1000 \mu F \; (preferred \; \; value \; \;)$$

Hence the value C1 = 1000uF.

The value of dt = 10ms for a frequency of 50Hz, full wave rectification, while the maximum current expected from the power supply is 0.3A.

C3 filters any noise at the output of the regulator.

3.2 SOLAR PANEL STAGE.

The choice of solar panel to be used depends largely on the capacity of the battery to be charged. From unit 1.1 above, we have estimated the worst case charging current for the mobile phone to be 2700mA. Hence for a 12V solar panel,

$$panel \; power = 12 \; X \; 0.27$$
$$= 3.24 \, W.$$

A 5W solar panel was used, since at low sunlight intensities proper charging is still required. The panel is connected to the regulator input via D1 (D1prevents reverse charging which could drain the battery if there is no sunlight). Fig 3.2a below shows the solar charging stage.

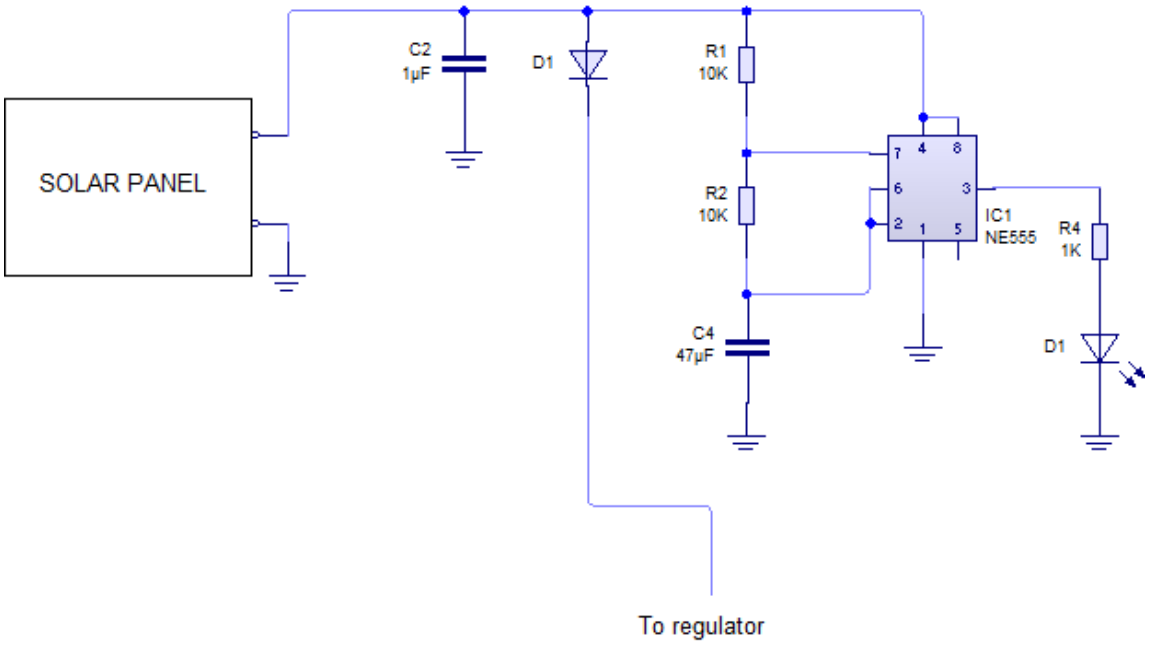


Fig 3.2 Solar Charging Stage.

IC1 is an astable 555 timer stage, which gives a blinking indicator, to indicate the solar panel is connected and giving output.

For the astable, the frequency is supposed to be approximately 1Hz to allow for an observable blinking rate. For the astable timer,

$$f = \frac{1.44}{(\ Ra + 2Rb\ )C} \text{ -------- where } f \text{ is frequency in Hz.}$$

From the diagram in fig 3.2a, Ra = R1 and Rb = R2, C = C4.

For F = 1Hz, set C= 47uF & Ra = 10K.

For the light emitting diode (D1),

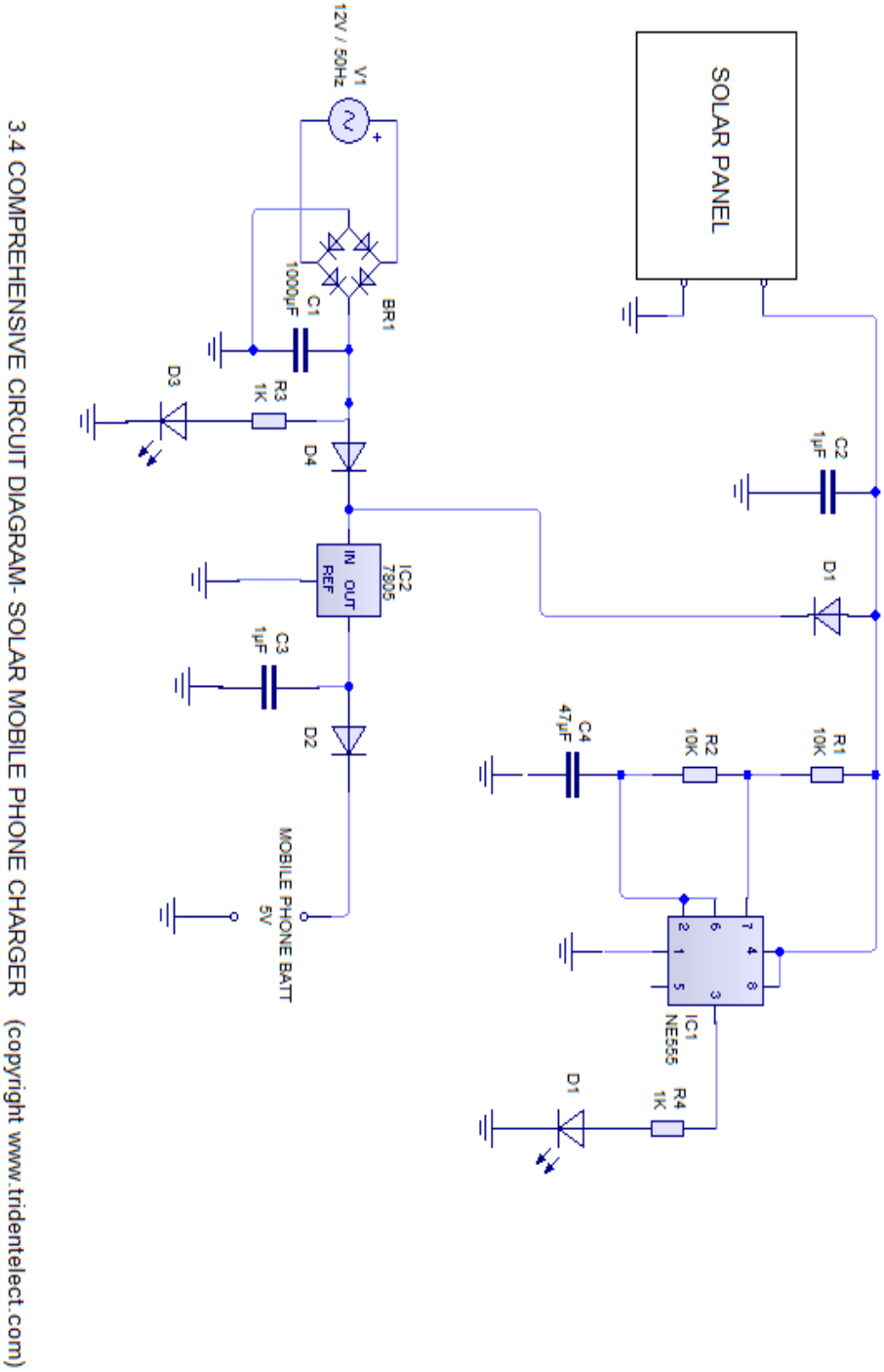
$$forward\ voltage\ (Vf = 1.7\ V\ ),\ forward\ current\ (If = 10mA\ ) - - from\ data\ sheets$$

$$hence\ R4 = \frac{(V+) - (Vf)}{If}$$

$$= \frac{10.3 - 1.7}{0.01} = 960\Omega$$
$$= 1K\ (preferred\ value\ )$$

V+ is 10.3 because the 555 timer output is Vcc – 1.7V. so for solar voltage (Vcc) of 12V, Vout = 10.3V.

From the above calculations R4 = R3 = 1KΩ.



3.4 COMPREHENSIVE CIRCUIT DIAGRAM- SOLAR MOBILE PHONE CHARGER (copyright www.tridentelect.com)

4. CONCLUSION

The design and analysis presented in this paper has shown clearly that mobile phone batteries can be charged, not only by alternating current mains supply, but more effectively by solar battery charger. Moreover, the ability and possibility of the photovoltaic solar cell to generate

electrical energy has been established and applied. Hence, it will be good to recommend this design for technical modification and implementation by various electrical and electronics engineering industries and also for domestic and office use to charge mobile phones.

REFERENCES

[1] J. G. Nielsen, M. Newman, H. Nielsen, and F. Blaabjerg, "Control and testing of a dynamic voltage restorer (DVR) at medium voltage level," *IEEE Transactions on Power Electronic* vol. Vol. 19 (3), pp. pp: 806–813 2004.

[2] R. Omar and N. A. Rahim, "New Control Technique Applied in Dynamic Voltage Restorer for Voltage Sag Mitigation," *4th IEEE Conference on Industrial Electronics and Applications,* pp. pp. 848-852, 2009.

[3] P. T. Nguyen and T. K. Saha, "Dynamic Voltage Restorer Against Balanced and Unbalanced Voltage Sags " *Modeling and Simulation IEEE 2004,* pp. pp.1-6, 2004.

[4] K. Perera, D. Salomonsson, A. Atputharajah, and S. Alahakoon., "Automated Control Technique For A Single Phase Dynamic Voltage Restorer," IEEE 2006.

[5] K. Agileswari, Ramasamy, R. K. Iyer, Dr.R.N.Mukerjee, and Dr.VignaK.Ramachandramurth, "Dynamic Voltage Restorer for voltage sag compensation," *IEEE PEDS, 2005, pg.1289-1293.*

[6] R. Omar, N. A. Rahim, and M. Sulaiman, "Modeling and simulation for voltage sags/swells mitigation using dynamic voltage restorer (DVR)," *Journal of Theoretical and Applied Information Technology, JATIT,* 2005 - 2009.

[7] C. Zhan, V. K. Ramachandaramurthy, A. Arulampalam, C. Fitzzer, M. Barnes, and N. Jenkins, "Control of a battery supported dynamic voltage restorer," *IEE proceedings on Transmission and Distribution,* pp. pp.533-542., 2002.

[8] T. Devaraju, V. C. Veera Reddy, and M. Vijaya Kumar, "Performance of DVR Under Different Voltage Sag and Swell Condition," *Asian Research Publishing Network,* p. pp. 56, 2010.

[9] E. H, S. A, T. M, and S. M.M., "Simulation of Dynamic Voltage Restorer Using Hysteresis Voltage Control," *European Journal of Scientific Research (EJSR),* pp. pp.152-166., 2009.

[10] H. P. Tiwari, "Capacitor Rating Selection for Voltage Sag Compensation in DVR System," *International Journal of Innovation, Management and Technology,* vol. Vol. 1, No. 3,, pp. pp. 295-299, 2010.

[11] P. Boonchiam and N. Mithulananthan, "Understanding of Dynamic Voltage Restorers through MATLAB Simulation," *Thammasat Int. J. Sc. Technology,* vol. Vol. 11, No. 3, July-Sept 2006.

[12] A. O. Ibrahim, T. H. Nguyen, and D.C. Lee, "A Fault Ride-Through Technique of DFIG Wind Turbine Systems Using Dynamic Voltage Restorers," *IEEE Transaction Energy Conversion,* vol. Vol. 26, No. 3, pp. pp. 871-882, Sept. 2011.

[13] K. Sandhya, L. Dr. A. Jaya, and D. M. P. Soni, "Design of PI and Fuzzy Controllers for Dynamic Voltage Restorer (DVR)," *AASRI conference on Power and Energy system,* 2012.

[14] J. Chiha, Ghabi, and N. Liouane, "TUNING PID CONTROLLER WITH MULTI-OBJECTIVE DIFFERENTIAL EVOLUTION," *Proceedings of the 5th International Symposium on Communications, Control and Signal Processing, ISCCSP 2012, Rome, Italy, 2-4* pp. pp 1-10, May 2012.

[15] B. Zuo and J. Li, "PID Controller Tuning by Using Extremum Seeking Algorithm Based on Annealing Recurrent Neural Network," *3rd International Symposium on Knowledge Acquisition and Modeling,* pp. pp 132-135, 2010

[16] Y. Zhang and J. Li, "Fractional-order PID Controller Tuning Based on Genetic Algorithm," *978-1-61284-109-0/11/©2011 IEEE,* pp. pp 764-767.

[17] www.tridentelect.com.

[18] http://en.wikipedia.org/wiki/Solar_energy