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DESIGN OF A NEW MODIFIED CLOCK GATED SENSE-AMPLIFIER FLIP-FLOP

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ABSTRACT

In this paper a new modified explicit-pulsed clock gated sense-amplifier flip-flop (MCG-SAFF) is proposed for low power and high performance applications. By embedding dual-edge triggering mechanism and conditional pre-charging in the new symmetric latch, the MCG-SAFF is capable to achieve low power dissipation and delay. The simulations are carried out in mentor graphics tools of 130nm technology. From this it is evident that with the proposed design there is 22.1% reduction in power dissipation and 76.5% in delay. When the switching activity is less than 0.5, the proposed MCG-SAFF shown its superiority in terms of power reduction. During zero input switching activity, MCG-SAFF can realize upto 86% in power saving.

Index Terms – Dual-edge triggering, Clock-gated, high performance, Low- power.

I. INTRODUCTION

Very - large - scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. In VLSI designs, the clock system that includes clock distribution network and flip-flops consumes 30% to 60% of the total system power, where 90% is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flops [1]. By utilizing the dual edge triggering the flip-flop is capable of sampling data on both rising and falling edges of the clock [2]. Many low-power and high speed flip-flop designs are available in open literature [3]-[10].
In this paper a new modified clock gated sense amplifier flip-flop is proposed.

II. REVIEW OF EXISTING FLIP-FLOPS

A. *Dual-Edge Triggered Sense-Amplifier Flip-Flop*

In Fig.1 the dual edge triggered pulse generator [12] is shown the schematic diagram of the DET-SAFF produces a pulse signal synchronized at the rising and falling clock edges. The pulse generator can be shared by multiple flip-flop circuits when a group of flip-flops are located closely. For a sense amplifier based flip-flop, in the evaluation phase, as soon as D is low, SB will be set to high, and if D is high, RB will be set to high. The sensing and latching stages of dual edge triggered sense amplifier flip-flop are shown in Fig.2.

Therefore, the conditional pre-charging technique is applied in the sensing stage of DET-SAFF, to avoid redundant transitions at major internal nodes.

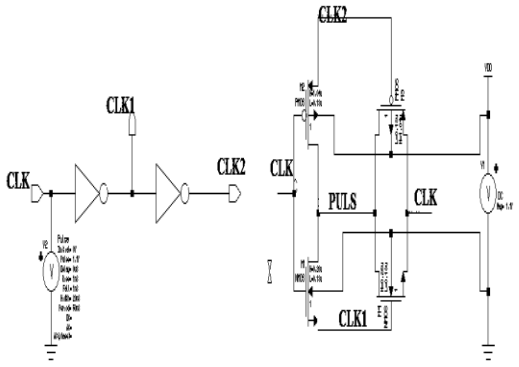


Fig.1.Dual pulse generator

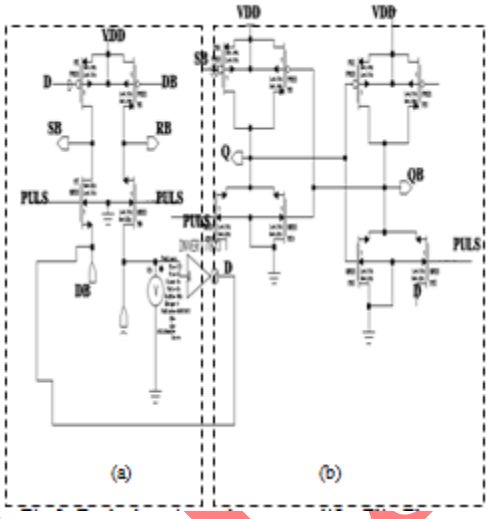


Fig.2. Dual edge-triggered sense-amplifier Flip-Flop:

(a) Sensing stage, and (b) Latching stage

Two input controlled PMOS transistors in the pull-up stage of sense amplifier are embedded in the pre-charge paths of nodes SB and RB, respectively. In this case, if D remains high for n cycles, SB may only be discharged in the first cycle. For the following cycles, SB will be floating when PULS is low or fed to the low state DB when PULS is high. As for RB, it only needs to be pre-charged in the first cycle and remains at its high state for the remaining cycles.

Since the pre-charging activity is conditionally controlled, the critical pull down path of SB and RB is simplified, consisting of only one signal transistor. This helps to reduce the discharging time significantly. As such, the resulting sensing stage possesses low-power and

high-speed features. A fast symmetric latch is developed; this new latch [13] makes use of SB and RB to pull up the output nodes. But the pull down path is modified. It composes PULS controlled NMOS pass transistor, through which D (DB) is directly fed to the Q (QB) node. This topology significantly speeds up the high-to-low output transition because the output latch immediately captures the input value once the PULS signal is generated. On the other hand, the low-to-high latency will also be improved. This is because the output node will not only be charged by the pull-up transistors[14], but also with the pull down pass transistors. The advantage of DET-SAFF is high speed and low power. But the unnecessary transitions especially at low switching activities cause a lot of power to be wasted.

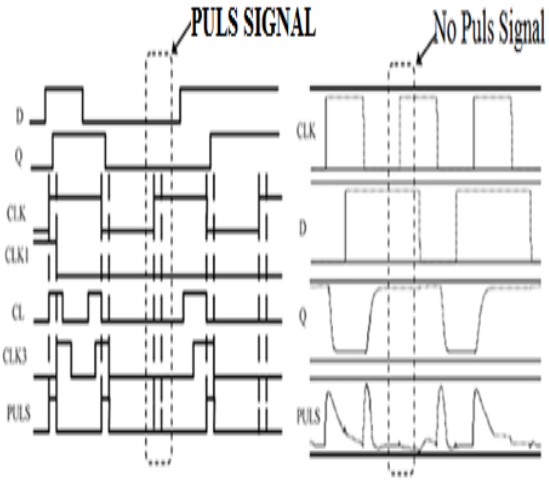
B. Clock-Gated Sense-Amplifier Flip-Flop

In order to eliminate the redundant transitions in the pulse generator, the CG-SAFF is constructed. It utilizes the DET-SAFF design as a baseline and incorporates the clock gating technique [15]. Clock gating is a technique used in many synchronous circuits for reducing dynamic power dissipation. Synchronous circuit is a digital circuit in which the parts are synchronized by a clock signal. In CG-SAFF, the clock gating technique is implemented by event.

The timing diagram and simulated waveform of the clock gated pulse generator is shown in Fig.3. The schematic of pulse generator is shown in Fig.4. In order to compare the previous and current input values, two comparators are used to produce signals X and Y, by using the differential inputs, D and DB, and the outputs, Q1 and QB1, as control signals. If D is different from the output Q1 of Q, X will be pulled up to high and Y to low.

Transistor N3 is turned on to allow the clock signal to pass through as CL (Gated clock). At the same time, P1 is ON and drive the CLK1 signal to high before the rising edge of the clock. Therefore, transistor N5 and the transmission gate are turned ON, driving the PULS signal to high. After a short period, the transparent window is closed as CLK1 goes low and CLK3 is pulled up. Thus, a short transparent period is created at the rising edge of the clock.

Note that signal CLK1 is used for pulse generation rather than CLK2. Such design aims to ensure that the flip-flop only captures the data at the triggering edge of the clock, thereby preventing race problems. At the falling edge of the clock, CL is low and CLK3 is high. The sampling window is shut down once CLK3 is low. When the input D remains the same in consecutive clock cycles, X is low and Y is high. CL is pulled down so that the flip-flop has shown its superiority in power dissipation at low switching activity, but the area occupied by the design is more.



(a) (b)

Fig.3. Clock-gated pulse generator: (a) Timing diagram; (b) Simulated waveform

The sensing and latching stage of CGSAFF is shown in Fig.5. The sensing stage is same as DET-SAFF it consists of modified Nikolic's latch [15] to hold buffered and differential outputs. The generated Q1 and QB1 instead of Q and QB are used in pulse generator to obtain the PULS signal. This design has shown it's superiority at low switching activity.

III. PROPOSED MODIFIED CLOCK-GATED SENSE AMPLIFIER FLIP-FLOP

The proposed modified clock gated sense-amplifier flip-flop of three stages: the pulse generating stage, sensing stage and the latching stage. The simple pulse generator and sensing stage used in proposed MCG-SAFF is same as that of CGSAFF [15]. The schematic diagram of the proposed MCG-SAFF is shown in Fig.6. The pulse generator samples data core that is based upon sense-amplifier flip-flop (SAFF); CLK and CLK3 both are high for a short period of time on the CLK rising edge, CL and CLK4 on the CLK falling edge. For this design a new high speed symmetric latch is developed. This new latch makes use of SB and RB to pull-up the output nodes. If the input D is high, RB will be set to high then both the transistors in the pull down network will conducts and a sharp discharge path is established from QB to Ground.

But at the same time node SB is set to low to turn on the pull up transistor and charges the output node Q to high state. The inner holding arrangement is modified to obtain buffered differential outputs, Q1 and QB1. This new arrangement speeds up the low to high output because the latch circuit immediately captures the input once the PULS is generated.

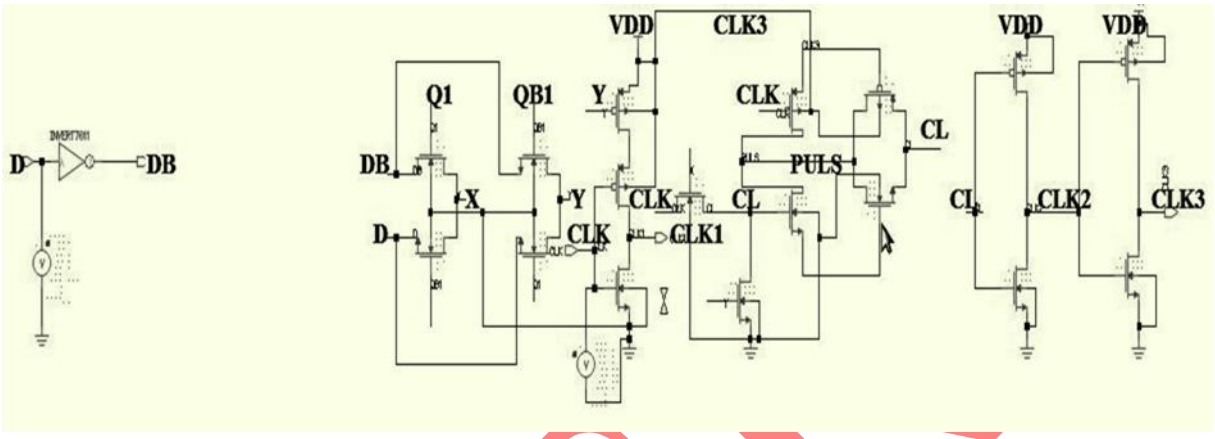


Fig.4. Schematic diagram of clock-gated pulse generator:

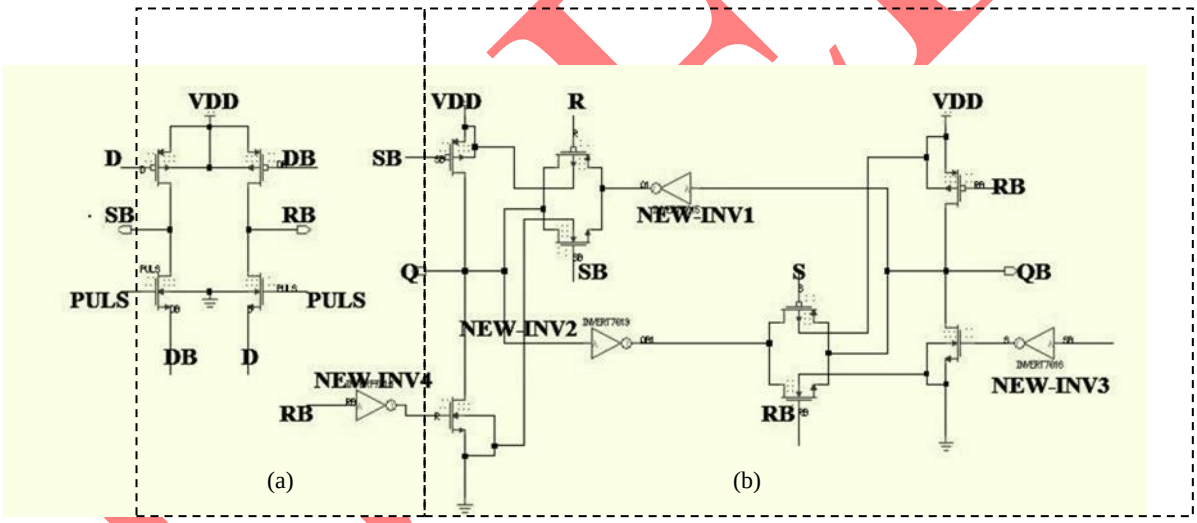
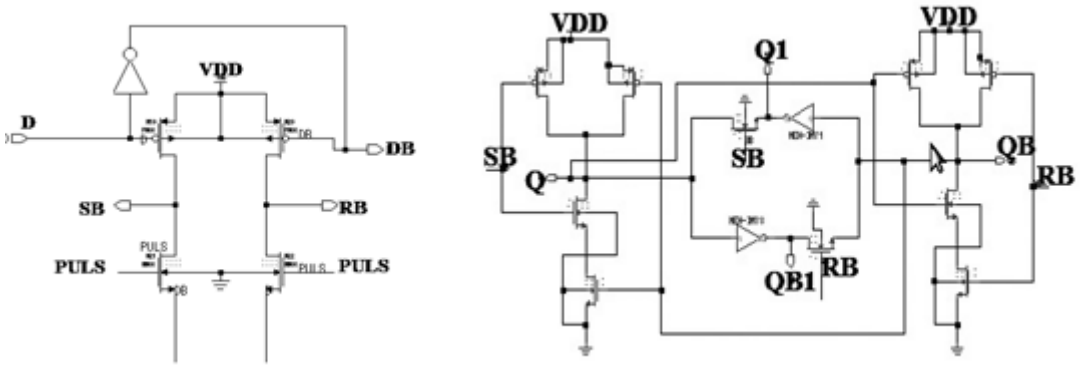


Fig.5. Clock-gated sense amplifier flip-flop (a) Sensing stage (b) Latch stage



(a) (b)

Fig.6. Proposed modified clock gated sense-amplifier Flip-Flop: (a) sensing stage, and (b) latching stage.

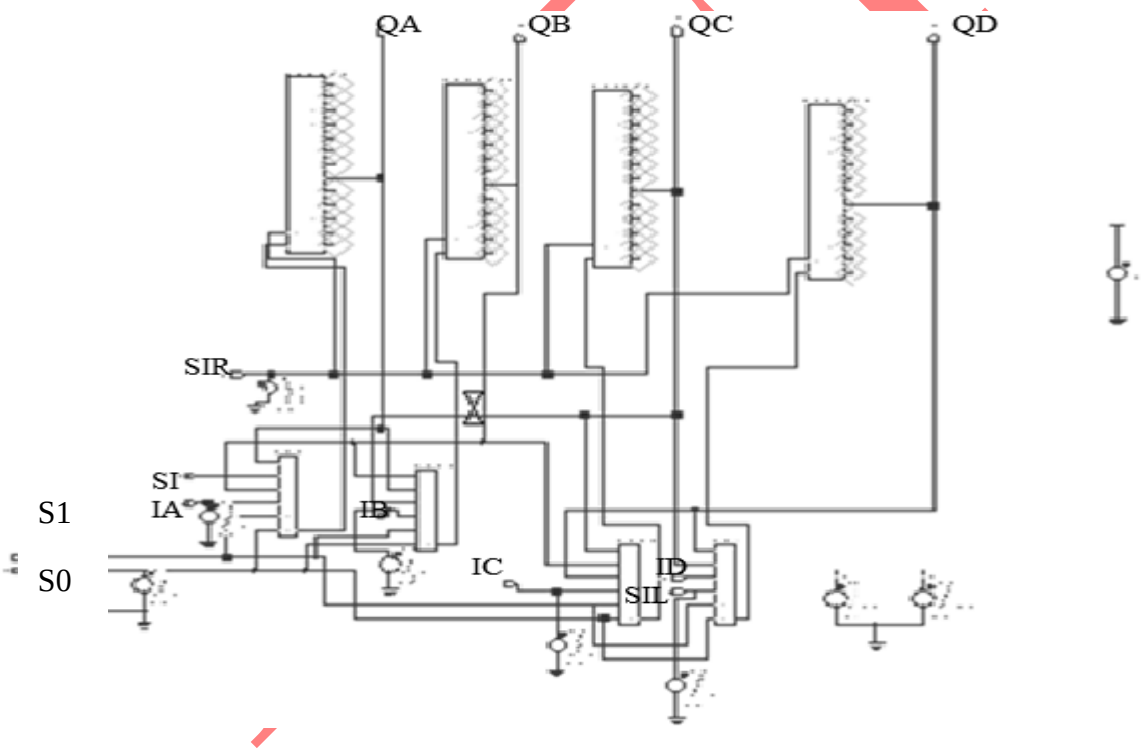


Fig.7. Universal shift register

An universal shift register is designed using proposed flip-flop as shown in Fig. 7. When the selection inputs of the universal shift register S1=0, and S0=0 then the shift register holds the previous state. If selection inputs as S1=0 and S0=1 then the register performs shift right operation by taking serial input (SIR). When inputs are S1= 1 and S0 = 0 shift left operation

will be performed, for the input S1=1 and S0=1 parallel input and parallel output operation will be performed.

IV. SIMULATION RESULTS AND PERFORMANCE COMPARISONS

These flip-flops were designed using Chartered Semiconductor Limited's 0.13-µm CMOS process technology, at an operating temperature of 27^0C and a supply voltage of 1.8V, using MENTOR GRAPHICS TOOLS. The design was optimized to 1.25 GHZ. The performance of the proposed flip-flop is evaluated by comparing with CGSAFF [15]. Table I-II shows the performance analysis of CG-SAFF and modified CG-SAFF. The proposed MCG-SAFF has the least CLK-to-Q delay among the simulated flip-flops. It achieves 76.5% reduction in delay. The relationship of CLK-to-Q delay with respect to the D-to-CLK delay is presented in Fig.8. Finally, Table III summarizes the comparison results of CG-SAFF and MCG-SAFF.

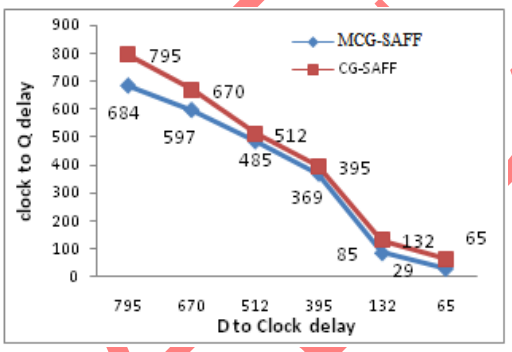


Fig.8. CLK-to-Q delay as a function of D-to-CLK delay.

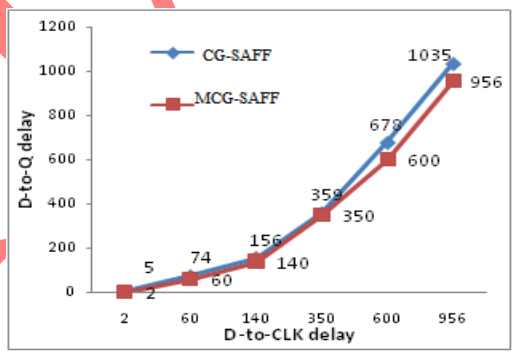


Fig.9. D-to-Q delay as a function of D-to-CLK delay.

TABLE I: PERFORMANCE ANALYSIS OF CG-SAFF @1.8V AT DIFFERENT OPERATING FREQUENCIES FOR DIFFERENT SWITCHING ACTIVITY

SWITCHING ACTIVITY (α)	MOCF (GHz)	D-Q delay (ps)	CLK-Q delay (ps)	RISE TIME (ps)	FALL TIME (ps)	TOTAL POWER DISSIPATION (nw)
25%	0.83	2647.2	642.23	1226.6	-	33.0154
	1.0	2548.1	543.13	1027.4	-	33.0154
	1.25	2051.2	446.18	829.49	-	33.0153
50%	0.83	2246.8	641.77	1226.0	213.24	33.0154
	1.0	2548.1	543.11	1027.5	235.89	33.0154
	1.25	2051.2	446.9	829.50	304.81	33.0154
75%	0.83	2647.2	642.23	1226.6	193.99	33.0154
	1.0	2548.1	543.12	1027.5	214.22	33.0154
	1.25	2051.2	446.19	829.50	340.29	33.0152
100%	0.83	2246.8	641.79	1226.0	212.19	33.0154
	1.0	2548.1	543.12	1027.5	214.22	33.0154
	1.25	1653.3	448.30	830.19	351.63	33.0154

TABLE II: PERFORMANCE ANALYSIS OF MCG-SAFF @1.8V AT DIFFERENT OPERATING FREQUENCIES FOR DIFFERENT SWITCHING ACTIVITY

SWITCHING ACTIVITY (α)	MOCF (GHz)	D-Q delay (ps)	CLK-Q delay (ps)	RISE TIME (ps)	FALL TIME (ps)	TOTAL POWER DISSIPATION (nw)
25%	0.83	1504.5	699.52	969.34	-	25.8345
	1.0	1606.2	601.20	98.571	-	25.8346
	1.25	1313.2	508.15	109.12	-	25.8345
50%	0.83	1104.2	699.18	95.445	44.877	25.8345
	1.0	1606.6	601.64	99.241	45.283	25.8345
	1.25	1313.1	508.15	109.16	47.043	25.8345
75%	0.83	1504.5	699.52	96.695	44.666	25.8345
	1.0	1606.1	601.13	98.452	45.299	25.8345
	1.25	1313.1	508.13	109.15	47.029	25.8329
100%	0.83	1104.1	699.11	95.295	44.742	25.8345
	1.0	1606.1	601.15	98.433	45.257	25.8331
	1.25	917.09	512.09	114.10	46.996	25.8345

TABLE III: COMPARISON RESULTS OF CG-SAFF AND MCG-SAFF

Designs	**CG - SAFF**	**MCG - SAFF**
CLK-to-Q delay(ps)	795	187.03
Min D-to-Q delay(ps)	1653.4	592.03
Rise time(ps)	830.27	79.809
Fall time(ps)	800	800
MOCF(GHZ)	1.25	1.25
# of transistors	40	38

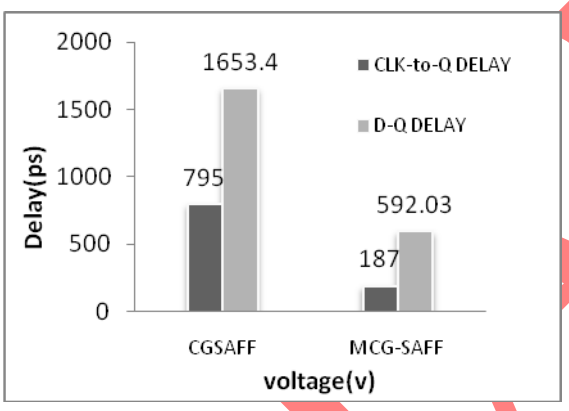


Fig. 10. CLK-to-Q delay as a function of D-to-Q delay.

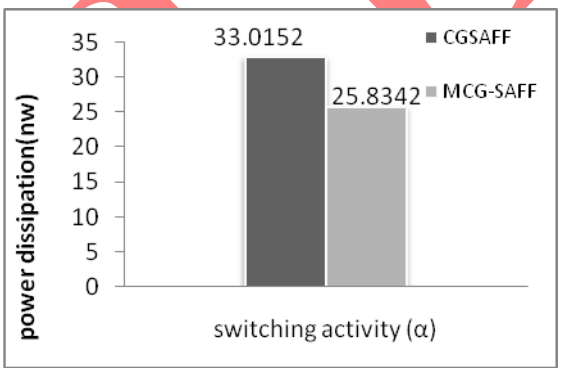


Fig. 11. Power dissipation of different flip-flops

V. CONCLUSION

In this paper modified clock gated sense amplifier flip-flop is presented which uses positive feedback is formed by cross coupling two bi-stable elements for low power and high performances applications. Due to the presence of clock-gated circuit in the pulse generator the design acquires large delay in the CLK-to-Q and D-to-Q mechanism in CGSAFF. But the MCG-SAFF circuit acquired 76% less delay than CGSAFF. This new design achieves substantial power reduction by incorporating dual-edge triggering and conditional pre-charging. It also minimizes latency by utilizing a fast latch. This new design is developed to reduce the power dissipation and delay when compared to the clock gated sense amplifier flip-flop up to 22.1% and 76.5% respectively.

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