BUILT-IN SELF-TEST AND CALIBRATION OF ON-CHIP SPECTRAL CHARACTERISTICS WITH LOW COMPLEXITY

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ABSTRACT-

This project presents built-in testing (BIT) architecture and its implementation for On-Chip Spectral characteristics to analyze with low complexity. It enables the frequency response and harmonic distortion characterizations of an integrated device-under-test (DUT) through reconfigurable coherent sampling rate. This accurate FFT analysis approach is based on coherent sampling, but it requires a significantly smaller number of points to make the FFT realization more suitable for on-chip built-in testing and calibration applications that require area and power efficiency. External analog instrumentation is avoided, reducing test time and cost. The proposed on-chip testing scheme use Fast Fourier Transform (FFT) algorithm with fixed size and a simple signal generator synchronized with a modified ADC resolution and the overall accuracy is limited by the ADCs resolution. A general methodology for the use of this structure in the functional verification of a DUT is also provided. The technique was assessed by comparing the simulation results from the proposed method of single and multiple tones with the simulation results obtained from the FFT of coherently sampled tones. The results indicate that the proper selection of test tone frequencies can avoid spectral leakage even with multiple narrowly spaced tones.

Keywords- Reconfigurable FFT architecture, radix-2kalgorithm, complex coherent sampling, multitone signals.

INTRODUCTION

Accurate frequency estimation of distorted and noisy signals in industrial power systems is a challenging problem that has attracted much attention. In power systems, the typical application of frequency estimation is for protection against loss of synchronism, under-frequency relaying, power-quality monitoring, and power system stabilization. De-noising and frequency recognition are of critical importance in practical deployment of signal communications. Many de- noising techniques exist in the literature. However, few of them are based on a general and rigorous framework, while at the same time demonstrating effectiveness in large-scale robust multi tone frequency recognition experiments. A key point of this work is to use of a strong on chip testing recognition model. The built in self-testing

algorithm incorporates prior knowledge about the structure of signals, noise model, which is essential to its performance.

A new method for frequency estimation technique is used in on chip built in self-testing. In any case, the accuracy of the frequency estimation provided by the FFT are affected by errors due to the wideband noise superimposed onto the acquired data in the practical applications. There is a necessity to investigate the statistical behavior of the frequency estimation of distorted and noisy harmonic signals provided by simple and accurate interpolation algorithm. The reason is given here.

1) The influence of a stationary white noise on the frequency estimation provided by the multipoint interpolation FFT based on the maximum side lobe decay window has been analyzed. The frequency estimations are based on the FFT which uses the direct ratio of two maximum amplitude spectral lines and thus contains even items.

RADIX -2K ALGORITHM

The N-point DFT is formulated as

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk}, k = 0,1,...N-1 \ldots..(1)$$

Where the twiddle factors is defined as $W_N^{nk} = e^{-\frac{2\pi nk}{N}}$ ..Here 'n' denotes the time index and the k denotes the frequency index. The radix 2^k algorithm can be derived by integrating twiddle factor decomposition through a divide and conquer approach.

A. Radix -2^2 Algorithm

Consider the first two steps of decomposition in radix-2 DIF FFT together. Applying a 3-dimensional linear index map as follows

$$n = \frac{N}{2} n_1 + \frac{N}{4} n_2 + n_3 \{n_1, n_2 = 0,1 n_3 = 0 \sim \frac{N}{4} - 1\} \ldots.(2)$$

$$k = k_1 + 2k_2 + 4k_3 \{k_1, k_2 = 0,1 k_3 = 0 \sim \frac{N}{4} - 1\}$$

The DFT has the form of

$$X(k_1 + 2k_2 + 4k_3) = \sum_{n_3=0}^{\frac{N}{4}-1} \sum_{n_2=0}^{1} \sum_{n_1=0}^{1} x(\frac{N}{2} n_1 + \frac{N}{4} n_2 + n_3) W_N^{nk}$$

This is also written as,

$$= \sum_{n_3=0}^{\frac{N}{4}-1} \sum_{n_2=0}^{1} \{B_{\frac{N}{2}}^{k_1}(\frac{N}{4} n_2 + n_3)\} W_N^{(\frac{N}{4} n_2 + n_3)(k_1 + 2k_2 + 4k_3)} \ldots(3)$$

where the first butterfly structure has the form of

$$B_{\frac{N}{2}}^{k_1}(\frac{N}{4}n_2+n_3)=x(\frac{N}{4}n_2+n_3)+(-1)^{k_1}x(\frac{N}{4}n_2+n_3+\frac{N}{2})\ldots(4)$$

Decomposing the composite twiddle factor, it can be expressed in Eq.(5).

$$W_N^{(\frac{N}{4}n_2+n_3)(k_1+2k_2+4k_3)}=(-j)^{n_2(k_1+2k_2)}W_N^{n_3(k_1+2k_2)}W_{N/4}^{n_3k_3}\ldots.(5)$$

Substituting the Eq.(5) into Eq.(3) and expanding the summation with regard to index n_2 ,we have a set of 4 DFTs of length $N/4$.

$$X(k_1+2k_2+4k_3)=\sum_{n_3=0}^{\frac{N}{4}-1}[H_{N/4}^{k_1k_2}(n_3)W_N^{n_3(k_1+2k_2)}]W_{N/4}^{n_3k_3}\ \ldots(6)$$

where a secondary butterfly structure $H_{N/4}^{k_1k_2}(n_3)$ is expressed as

$$H_{N/4}^{k_1k_2}(n_3)=B_{\frac{N}{2}}^{k_1}(n_3)+(-1)^{k_2}(-j)^{k_1}B_{\frac{N}{2}}^{k_1}(n_3+\frac{N}{4})\ldots.(7)$$

After these two columns, full multiplications are used to apply the decomposed twiddle factor $W_N^{n_3(k_1+2k_2)}$ in Eq.(6).Applying this cascade decomposition recursively to the remaining DFTs of length $N/4$ in Eq.(6), the complete radix -2^2 FFT algorithm is obtained. Equation (7) represents the first two columns of butterflies with only trivial multiplication of (-j) which can be implemented using only real-imaginary swapping and sign inversion.

The radix-2^2 algorithm is characterized according to the merit that it has the same multiplicative complexity and as the radix-4 algorithm, but still retains simple structures of the radix-2 butterfly.

B. Radix-2^3 Algorithm

To derive the radix-2^3 algorithm, the first three steps in cascade decomposition are considered. The linear index mapping transforms into 4-dimensional linear index maps,

$$n=\left\langle\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+n_4\right\rangle_N\ldots.(8)$$
$$k=\langle k_1+2k_2+4k_3+8k_4\rangle_N$$

Applying 4-dimensional linear index map to Eq.(1)

$$X(k_1+2k_2+4k_3+8k_4)=\sum_{n_4=0}^{\frac{N}{8}-1}\sum_{n_3=0}^{1}\sum_{n_2=0}^{1}\sum_{n_1=0}^{1}x(\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+n_4)W_N^{nk}\ \ldots.(9)$$

with the cascade decomposition, the twiddle factor can be expressed in the form of

$$W_N^{(\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+n_4)(k_1+2k_2+4k_3+8k_4)} = (-1)^{n_1k_1}(-j)^{n_2(k_1+2k_2)}W_8^{n_3(k_1+2k_2+4k_3)}W_{N/8}^{n_4k_4} \quad \ldots.(10)$$

Substitute Eq.(10) into Eq.(9) and expand the summation with regard to index n_1, n_2 and n_3,a set of 8 DFTs of length $N/8$ is identified.

$$X(k_1+2k_2+4k_3+8k_4) = \sum_{n_4=0}^{\frac{N}{8}-1}[T_{N/8}^{k_1k_2k_3}(n_4)W_N^{n_4(k_1+2k_2+4k_3)}]W_{N/8}^{n_4k_4} \quad \ldots.(11)$$

Where the third butterfly has the expression of

$$T_{N/8}^{k_1k_2k_3}(n_4) = H_{N/4}^{k_1k_2}(n_4)+(-1)^{k_3}W_8^{(k_1+2k_2)}H_{N/4}^{k_1k_2}(n_4+\frac{N}{8}) \ldots.(12)$$

Equation (12) reveals that the butterfly contains twiddle factors with $W_8^{(k_1+2k_2)}$.Since they are a constant scalar with $(-j)^{k_2}(\frac{\sqrt{2}}{2}(1-j))^{k_1}$ a constant multiplier can be used instead of a programmable multiplier such as the Booth multipliers. Full complex multiplications are used to apply the decomposed twiddle factor, $W_N^{n_4(k_1+2k_2+4k_3)}$, after the third column. The complete algorithm can be obtained by repeating the procedure.

PROPOSED ARCHITECTURE

In this brief, reconfigurable radix- FFT architecture is proposed. The proposed architecture consists of butterfly units, signal generator, coherent sampling (ADC), FFT block, calibration and spectrum analyzers.

BLOCK DIAGRAM

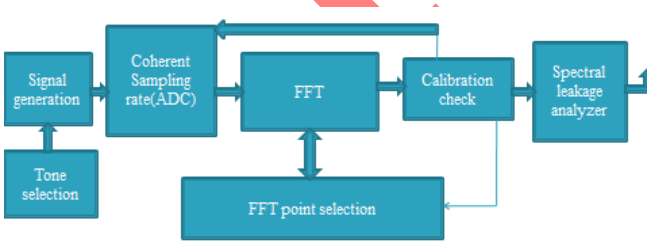


Fig.1 Block diagram of proposed system

A.Butterfly Units

The butterfly units perform complex additions and subtractions of two input data: $x(n)$ and $x(n+\frac{N}{2})$. The behavior of the butterfly units is as follows. All input values are saved into the delay buffers until the $\frac{N}{2}^{th}$ input is entered. Then, the butterfly units conduct calculations between the input values and delay buffer outputs, after entering the $(\frac{N}{2})+1^{st}$ input. During the last $\frac{N}{2}$ clock cycles, all butterfly calculations are performed at each stage. Butterfly unit 1 (BU1) conducts complex additions and subtractions only. However, butterfly unit 2 (BU2) includes twiddle factor W_4 multiplication utilizing the multiplexers and control signals.

B . Coherent sampling

In fig.2,the Coherent sampling is a useful and efficient technique for evaluating the spectral efficiency of analog/mixed signal circuits, because it increases the FFT accuracy and eliminates the need for a window function if certain conditions are met. Coherent sampling of a single tones assures that it's power in the spectrum is contained exactly one frequency bin. The condition for coherent sampling is given by,

Fin/Fsample = Ncycle/NFFT …… (13)

Where Fin is the input frequency, Fsamp is the sampling frequency, Ncycle is the integer number of cycles in the signal to be sampled, and NFFT is the length of the FFT engine.

To ensure coherent sampling, one can first determine the number of integer cycles that fits into the predefined sampling window, and use it to approximate the input frequency to the near optimal frequency that is exactly matches with one of the discrete frequency bin in the spectrum for the given FFT length.

Coherent sampling methods can be used for performing single-tone testing,

Because the nearby optimal frequency can be calculated by single tone frequency component. The proper selection of test tone frequencies can avoid spectral leakage even with multiple narrowly spaced tones. It follows the rules of coherent sampling instead of defining the near-optimal fundamental FFT frequency for a single test tone.

SIMULATION AND IMPLEMENTATION

VERILOG is frequently used for two different goals: simulation of electronic designs and synthesis of such designs. Synthesis is a process where a VERILOG is compiled and mapped into an

implementation technology such as an FPGA or an ASIC. Many FPGA vendors have free tools to synthesize VERILOG for use with their chips, where ASIC tools are often very expensive.

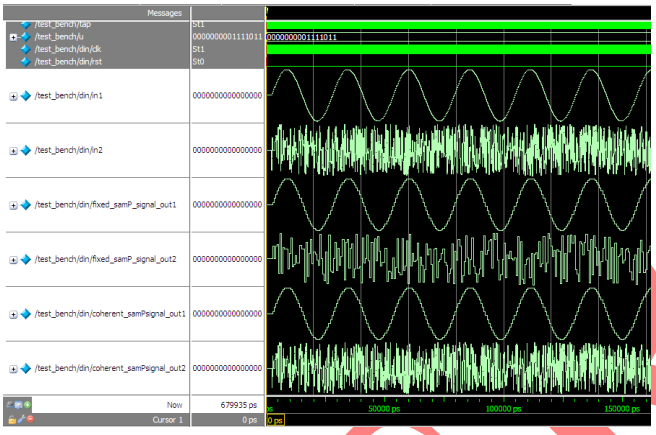


Fig.2.Coherent Sampling Output's

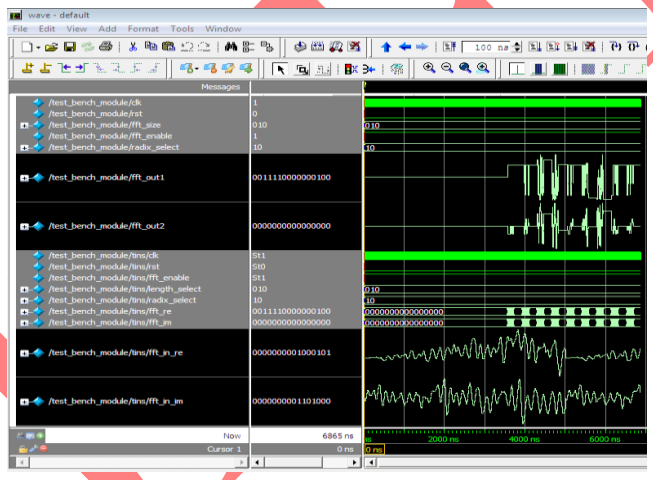
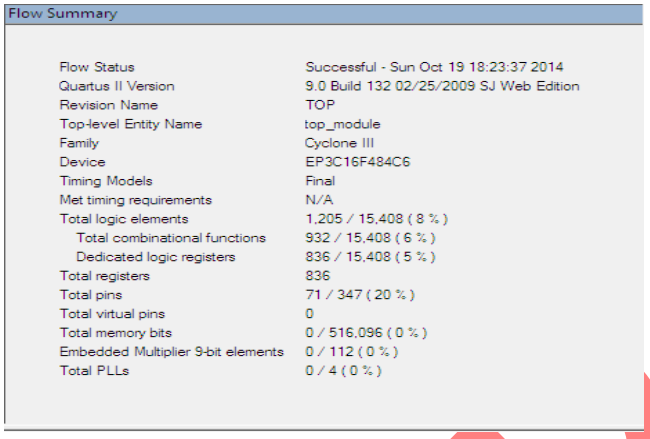


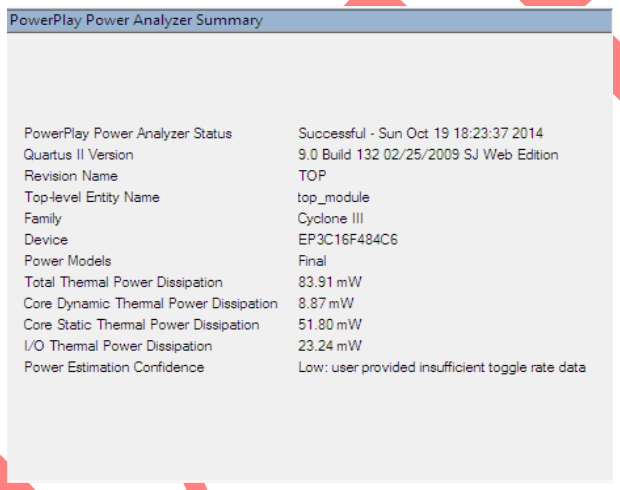
Fig.3.FFT with Fixed point Samples



Flow Summary

Flow Status	Successful - Sun Oct 19 18:23:37 2014
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	top_module
Family	Cyclone III
Device	EP3C16F484C6
Timing Models	Final
Met timing requirements	N/A
Total logic elements	1,205 / 15,408 (8 %)
Total combinational functions	932 / 15,408 (6 %)
Dedicated logic registers	836 / 15,408 (5 %)
Total registers	836
Total pins	71 / 347 (20 %)
Total virtual pins	0
Total memory bits	0 / 516,096 (0 %)
Embedded Multiplier 9-bit elements	0 / 112 (0 %)
Total PLLs	0 / 4 (0 %)

Fig.4.Area Utilization Report



PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Sun Oct 19 18:23:37 2014
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	top_module
Family	Cyclone III
Device	EP3C16F484C6
Power Models	Final
Total Thermal Power Dissipation	83.91 mW
Core Dynamic Thermal Power Dissipation	8.87 mW
Core Static Thermal Power Dissipation	51.80 mW
I/O Thermal Power Dissipation	23.24 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig.5.Power Utilization Report

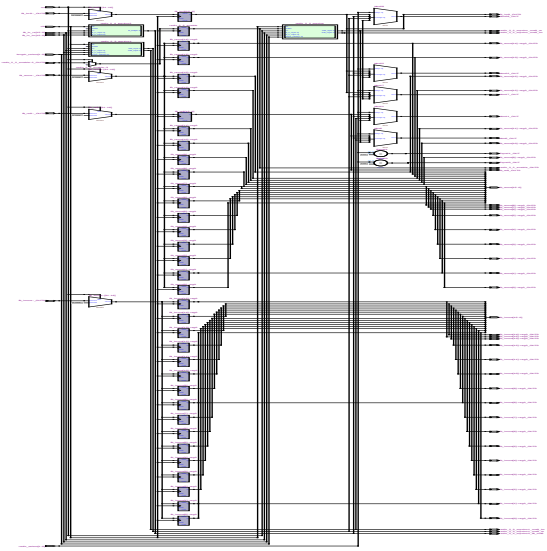


Fig .6.Hardware Implementation of Coherent Sampling FFT output's.

CONCLUSION

In this paper, a radix -2^k algorithm and coherent sampling based FFT will give better hardware complexity & power optimization with considerable delay enhancement. An accurate FFT-based analysis approach was introduced for FFT core with single and multitone point spectral characterizations. The project approach was derived from the coherent sampling method. The method avoids the use of a large number of FFT points to minimize the required FFT resources for area- and power-efficient built-in testing applications. *Modelsim* based pre simulation results of an FFT implementation showed the feasibility of the approach. For a QUARTUS II based hardware synthesis report of 16-point FFT computation, the implemented FFT engine consumes an estimated power of 77.10 mW and occupies an area of 256 nm which almost 4 times less as compared to variable point FFT .

An accurate FFT analysis based approach was introduced for on-chip spectral characteristics of multi tone signals. By selecting the appropriate frequency, ADC resolution and FFT length to achieve the desired frequency resolution in the output spectrum without the spectral leakage. This method avoids the use of large number of FFT points to minimize the on-chip FFT resources for area and power efficient applications.

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