DESIGN OF HIGH DRIVE BICMOS INVERTER AND NAND GATE FOR LOW POWER APPLICATIONS

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ABSTRACT

BICMOS technology is an emerging technology since it exploits both the advantages of CMOS and BIPOLAR, all the Intel [1] Pentium processors used the BICMOS technology. Compare to CMOS technology BICMOS technology manufacturing [2] process is difficult and costly that is the reason BICMOS technology is[3] not having that much of popularity as compare to CMOS technology. Here an attempt is made to design a high drive BICMOS device which consumes less power compared to conventional BICMOS technology. A NOVEL PMOS and NMOS is used in place of conventional PMOS and NMOS, Novel BICMOS has less Delay and high speed, and average power, delay calculated for both 45nm and 90nm technology.

Keywords: BICMOS Inverter, Merged BICMOS, Masking, Additional Process, Intel Processor

INTRODUCTION

Now a days BICMOS is becoming popular, BICMOS technology marries both BIPOLAR and CMOS on the same chip to extract the best[4] from both the technologies, the deficiency of MOS technology is limited load driving capabilities due to limited current sourcing and current sinking of both P and N transistors, the merits[5] of CMOS is Low power and high digital density and BIPOLAR having capacity to deliver large drive currents and rapidly charge heavy loads these advantages are the key factors for BICMOS technology[6], but in BICMOS technology involves high production cost(additional process and additional masking steps are required), large process time and process complexity, in general BIPOLAR is faster than CMOS technology since[7] it has high Trans conductance, different types of BICMOS technologies are available like medium speed and Low cost BICMOS, high cost high performance BICMOS and Merged BICMOS process[8]. Today's BICMOS technology must fulfill the requirements and should be compatible[9] with existing libraries and methodologies in ultra deep submicron region.

2.CONVENTIONAL PMOS AND NMOS

In Fig 1 and Fig 2 Conventional PMOS and NMOS's are shown the PMOS is good transfer of '1' and NMOS is good transfer of '0',in the digital or Analog or Mixed signal design The

PMOS and NMOS are basic elements in the design environment.

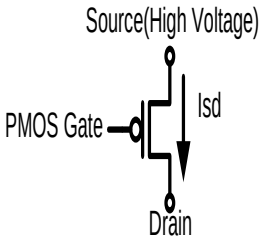

Figure 1:Conventional PMOS

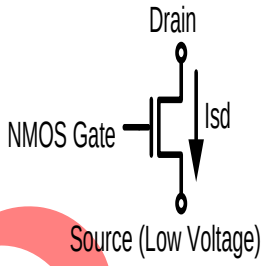

Figure 2:Conventional NMOS

3.DEMERITS OF CONVENTIONAL PMOS AND NMOS:

1.High delay
2.High leakage in Deep Submicron technology

4.PROPOSED PMOS AND NMOS:

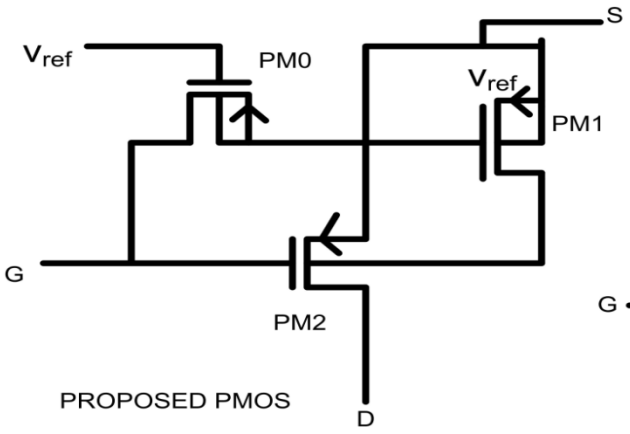

Figure 3:Proposed PMOS

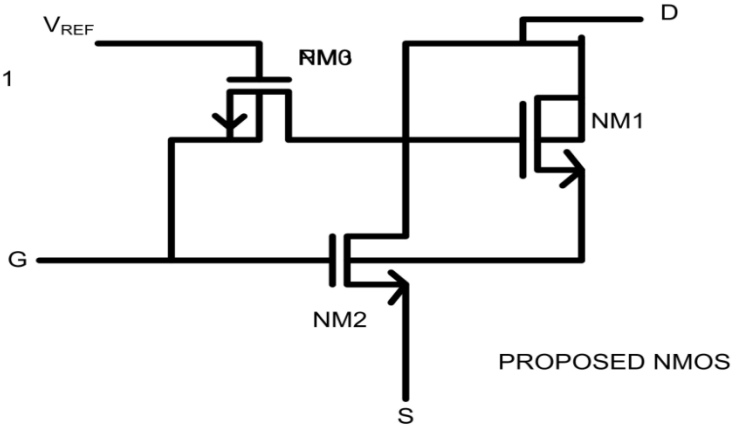

Figure 4:Proposed NMOS

Fig 3 and Fig 4 are proposed PMOS and NMOS having less delay and low leakage in deep submicron technology

4.1 working of Proposed PMOS and NMOS: in figure 3 for top transistor (PM0) a reference voltage of 0.8 v is applied, and input is applied to the gate terminals of bottom transistor (PM2) and output is taken across the drain terminals of the right transistor (PM1).[11]

5.BIPOLAR JUNCTION TRANSISTOR:

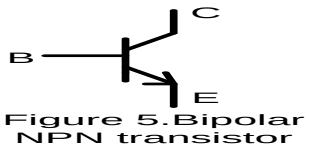

Figure 5.Bipolar NPN transistor

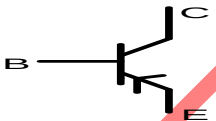

Figure 6.Bipolar PNP transistor

Figure 5:NPN Transistor Figure 6:PNP Transistor

Fig 5 & Fig 6 are NPN and PNP BIPOLAR JUNCTION Transistor,BIPOLAR JUNCTION transistors have high trans conductance and can drive high loads.

Therefore Designers want to exploit the advantages of CMOS[10] which has high input impedance,ideal switch and high density and BIPOLAR JUNCTION transistors have high[11]trans conductance which can be used to drive high loads,designers want to exploit the advantages of both CMOS and BIPOLAR JUNCTION transistor on the same chip, BJT can be used at load side and CMOS can be used at input side

6.CONVENTIONAL BICMOS INVERTER

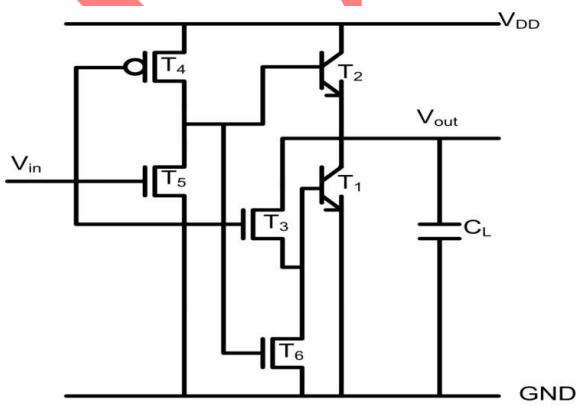

FIGURE 7:Conventional BICMOS inverter

FIG 7 is a conventional BICMOS inverter using conventional PMOS and NMOS simulated using CADENCE VIRTUOSO DESIGN environment at 45nm technology and simulated output is shown in FIG 8

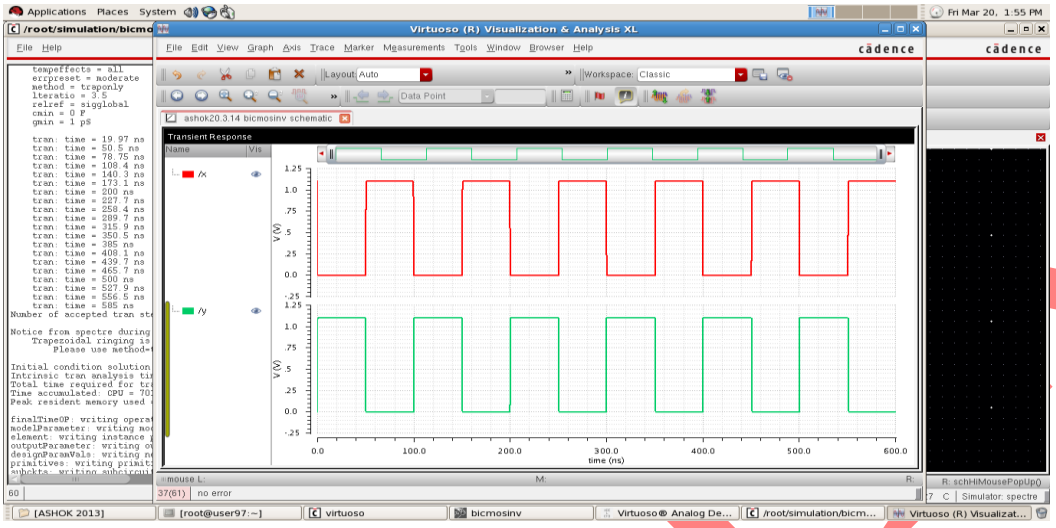

FIG 8 Conventional BICMOS inverter output

7.PROPOSED BICMOS INVERTER

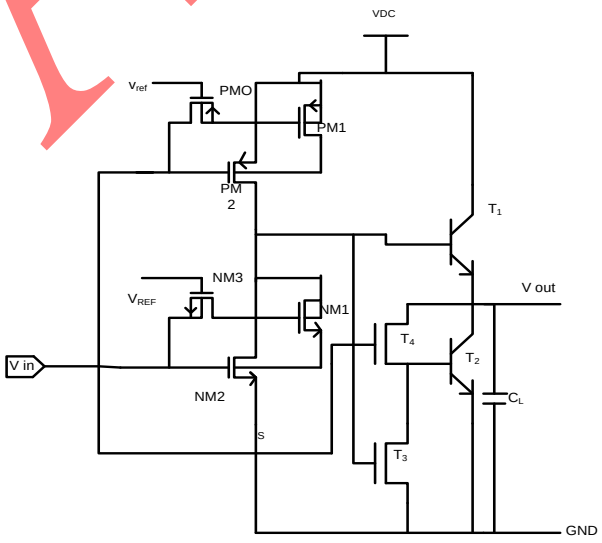

Figure 9 Proposed BICMOS inverter

In Fig 9 inplace of Conventional PMOS and NMOS a proposed PMOS and NMOS is used and simulated, simulated output is shown in FIG 10

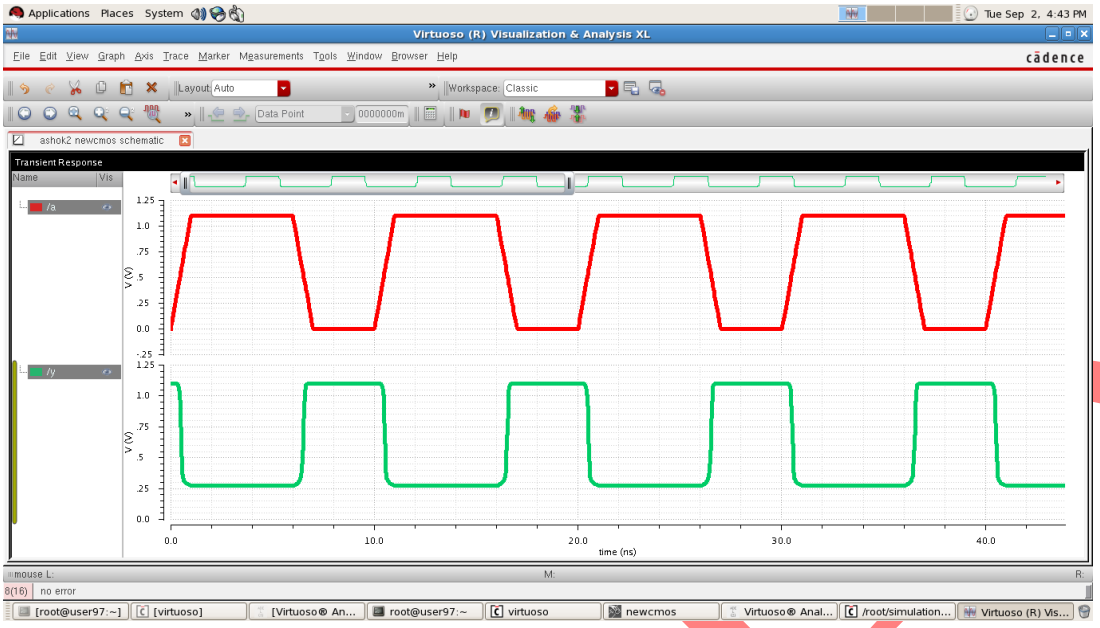

Figure 10 Proposed BICMOS inverter output

Both Conventional BICMOS inverter and Proposed BICMOS inverter average power, Delay and PDP values are calculated using Cadence Virtuoso Design tool at 45nm technology, the values are shown in Table1.1

TABLE : COMPARISON TABLE FOR CONVENTIONAL BICMOS NOVEL BICMOS.INVERTERS

Sl. No.	Technique	Power	Delay	PDP
1.	BICMOS INVERTER	2.55×10^{-6}	2.3×10^{-9}	5.86×10^{-15}
2.	PROPOSED BICMOS INVERTER	2.43×10^{-6}	1.9×10^{-9}	4.6×10^{-15}

From the table it is observed that proposed BICMOS inverter have less PDP value compare to conventional BICMOS inverter

8.CONVENTIONAL BICMOS NAND GATE

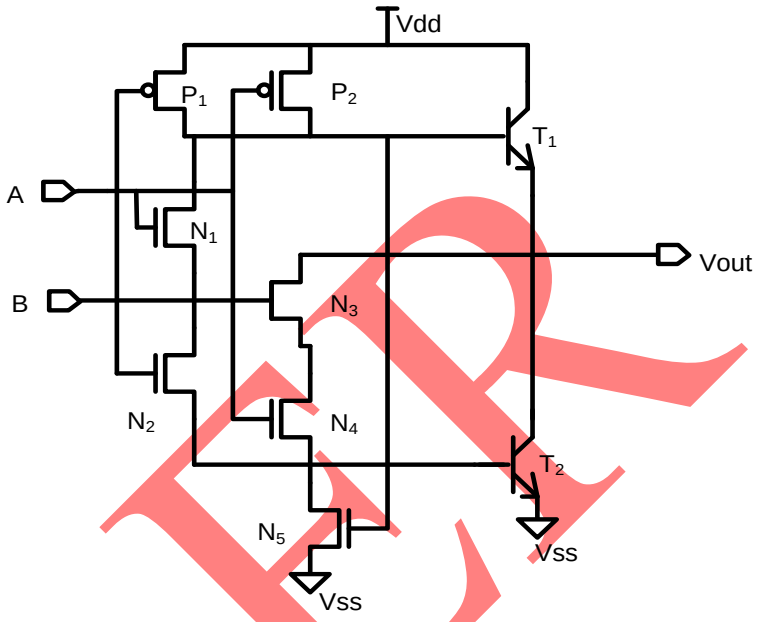

Figure 11 Conventional BICMOS NAND Gate

Fig 11 shows Conventional BICMOS NAND gate and simulated outputs are shown in Fig 12

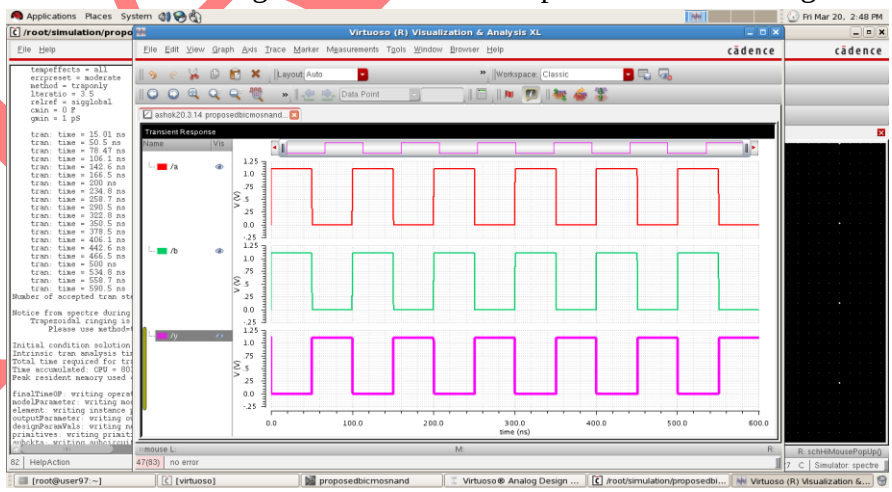

Figure 12 Conventional BICMOS NAND GATE output

9.PROPOSED BICMOS NAND GATE

Figure 13 is the proposed BICMOS NAND gate simulated using Cadence Virtuoso Designment Environment and simulated output is shown in Fig 14,average power,delay and PDP values are calculated and shown in table1.2

TABLE 1.2: COMPARISON TABLE FOR CONVENTIONAL BICMOS AND NOVEL BICMOS NAND NAND GATE.

Sl. No.	Technique	Power	Delay	PDP
1.	BICMOS NAND Gate	1.73×10^{-6}	3.5×10^{-9}	6.055×10^{-15}
2.	Proposed BICMOS NAND Gate	1.73×10^{-6}	3.9×10^{-9}	5.57×10^{-15}

From table 1.2 Proposed BICMOS NAND gate has low PDP value compared to Conventional BICMOS NAND gate

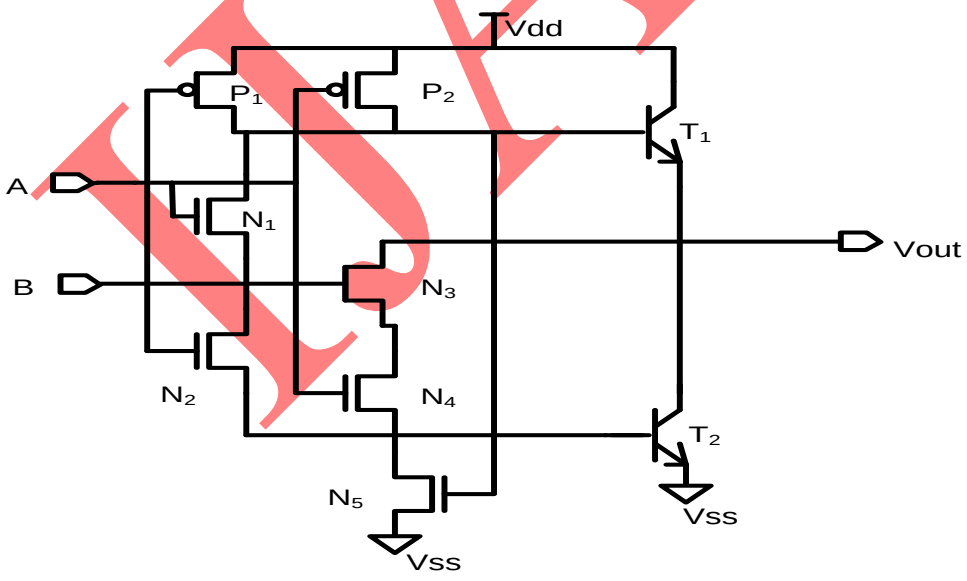

Figure 13 Proposed BICMOS NAND GATE

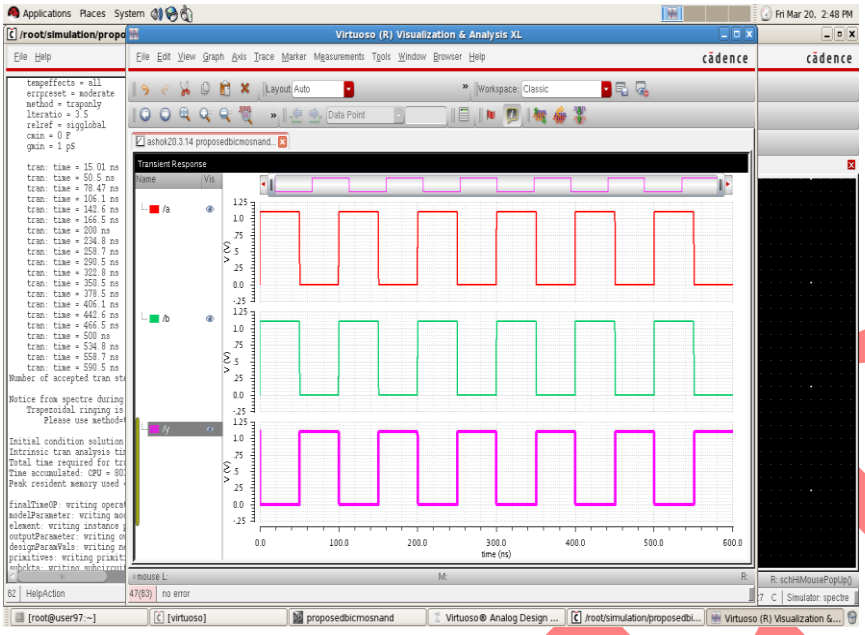

Figure 14: proposed BICMOS NAND GATE

10.CONCLUSIONS

We designed a Novel PMOS and NMOS with their use designed Novel BICMOS inverter and compared their PDP with conventional BICMOS inverter. In the same way we compared conventional BICOMS NAND with Novel BICMOS NAND. It is concluded that the proposed BICMOS inverter and proposed NAND gate have better power delay product with Conventional BICMOS inverter and Conventional BICMOS NAND Gate.

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