DESIGN AND EVALUATION OF WI-MAX TRANSCEIVER USING MPSOC

ERIC VIDHYA DHARAN.P , RAGAVENDRAN.U,
Department of Electronics and Communication Engineering,
SRM University, Chennai, India

ABSTRACT

Advancement in the field of communication has led to high speed data transfer in many audio and video applications at affordable rates. Wireless Interoperability for Microwave Access is one the technology that is used for this purpose. It includes the process of compressing, modulating the signal, Inverse Fourier Transform and cyclic prefix addition at the transmission end. It also includes the cyclic prefix removal, Fourier Transform, demodulation of the signal and decompression at the receiver end. The compression ratio and the signal to noise ratio is also found. In this paper, all the process involved in the design of W-Max Transceiver is discussed. Here, a framework that proposes energy mapping techniques such as task and core mapping is also discussed and the results are compared. All the components used in this Wi-Max Transceiver are modelled using Verilog HDL and the processing unit (PU) type used is the Nios II Processor. The area and the maximum frequency is obtained using Quartus II software.

I . INTRODUCTION

Miniaturization of electronic components has led to the introduction of complex electronic systems which are integrated onto a single chip, so-called systems-on-a-chip (SoCs)[1]. At the same time, performance requirements are increasing. The required performance of the system cannot be done by single processor systems. If achievable at all, this performance would come with an enormous power consumption and serious cooling problems, due to the necessity of very high clock speed. Currently, we can achieve the necessary performance by using several processors with moderate [3] clock speeds. Thus, many of the available SoCs contain several processors, which make them multiprocessor systems on a chip (MPSoCs). Thus, due to the involvement of many processors, this MPSoC architecture can be used for many applications. So the energy consumption may be high. But, they can be reduced to a greater extent by optimizing the tasks performed by the blocks and the positions of the blocks in the MPSoC architecture,.. There are several optimization techniques available for this process. The techniques include Simulated Annealing Algorithm, CPLEX solution, Energy Aware Mapping etc.

The energy consumption will include static energy, dynamic energy, re-configurable energy and communication energy [1]. Previously, only static and dynamic energy was considered in Mapping technique. Thus, we propose a heuristic that considers both re-configurable energy and communication energy. Then, the MPSoC architecture will be

obtained from task mapping and core mapping techniques. The proposed heuristic is used in implemented in a Worldwide Interoperability for Microwave Access (Wi-Max) Transceiver and its performance is evaluated.

High speed internet access at affordable cost has attracted huge number of users. In this present situation, Worldwide Interoperability for Microwave Access (WiMAX) have emerged as a low cost solution to broadband access [4]. The long range transmission with both high bandwidth (BW) and data rate makes WiMAX an obvious choice for industry applications. The IEEE 802.16e standard has introduced the subscriber's mobility, improving the capability of a wireless network. Better spectrum utilization is assured by adopting OFDM technology in physical layer design. The design of the Wi-Max Transceiver is as follows.

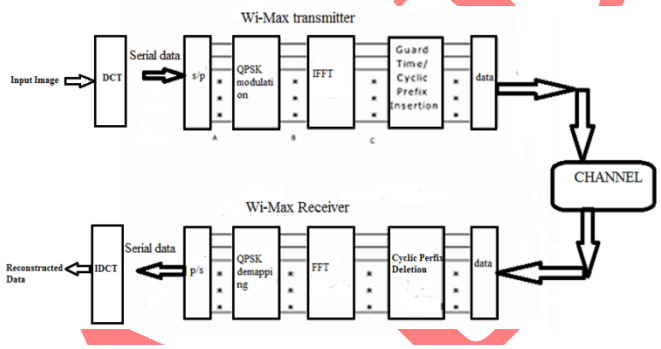

Fig 1. Wi-Max Transceiver

II . WI-MAX TRANSCEIVER

The word Wi-MAX is an acronym for "Worldwide Interoperability for Microwave Access" [10], It is a broadband Fixed Wireless Access system with the goal of delivering portable and mobile wireless connections on a metropolitan scale. It has been designed for point-to multipoint operation,(i.e) between one base station (BS) and several subscriber stations (SS). The specifications for both fixed Line of sight (LOS) communication are in the range of 10-66 GHz (IEEE 802.16c), and fixed, portable, non-LOS communication are in the range of 2-11 GHz (IEEE 802.16d & IEEE 802.16a). WiMAX is unique because of its design. Its design can deliver maximum throughput to maximum distance while offering 99.99 % reliability [10]. The block diagram of Wi-Max Transceiver is shown below.

WiMAX OFDM PHY:

Wi-Max OFDM is a multicarrier transmission scheme The information can be transmitted on multiple subcarriers, The carriers can be divided into three types:

- Data carriers for data transmission.
- Pilot carriers for various estimation purpose.

- Null carriers no transmission at all, for guard bands and DC carrier.

The implementations of Wi-MAX is different from OFDM PHY. The Fixed WiMAX, which is based on IEEE 802.16-2004, uses a 256 FFT-based OFDM PHY. Mobile WiMAX, which is based on the IEEE 802.16e-2005 standard, uses a scalable OFDMA-based PHY with FFT sizes from 128 to 2048.

WI-MAX TRANSMITTER

The functional blocks which compose the WiMAX transmitter are shown above [12]. The Data Units are fed into the DCT block to compress the data. Then the output is fed to the serial to parallel convertor to convert the serial bits into parallel bits. Then, the obtained bits are spreaded using the spreader. Then the data is interleaved by interleaver and mapped into symbol. Afterwards, the mapped data enter into the OFDM modulation which consist of assemble OFDM frame, 256 IFFT and cyclic prefix insertion. Then the data is transmitted over a channel. Data is fed in the form of image to matlab to convert to hexadecimal values. Then these values are given as input to modelsim for further process involved in transmission.

WI-MAX RECEIVER

The functional blocks which compose the WiMAX receiver as shown in the figure are the reverse functional blocks of WiMAX transmitter [12]. The received data coming from a channel is fed into the OFDM demodulation, which consist of removal of CP, Fast Fourier Transform (256 FFT) and disassemble OFDM frame. Then, the data demapping is performed by de-mapper and afterwards the demapped data enter the channel decoder. Channel decoder consists of de-interleaver, deseperator. The final block in receiver is the parallel to serial convertor that is used to convert the obtained parallel output into serial data. Then we can do IDCT to extract the compressed data. After decompressing the data, the .txt file that was generated from IDCT will be fed to Matlab to reconstruct the original image.

III . PERFORMANCE RESULTS

DISCRETE COSINE TRANSFORM (DCT)

Discrete Cosine Transform (DCT) is a lossy compression scheme in which a NxN image block is transformed from the spatial domain to the DCT domain. DCT decomposes the signal into DCT coefficients which are spatial frequencies components. The lower frequency DCT coefficients appear toward the upper left-hand corner of the DCT matrix and the higher frequency coefficients are in the lower right-hand corner of the DCT matrix. The

high frequency components will be removed to achieve compression. This method is followed in both row-wise and column-wise of the matrix to obtain 2D-DCT. Thus the data will be compressed more. Compression ratio is the ratio between the uncompressed size and the compressed size. Here, the compression achieved is 17.8 and Signal to Noise ratio is 2.1db. For the original image shown below, the obtained output of DCT is as follows.

Fig 2. Original Image

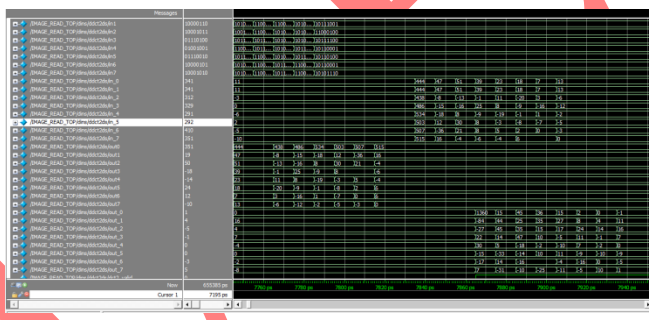

Fig 3. DCT

SERIAL TO PARALLEL CONVERTER

Input data is fed serially. Once the data has been clocked in, it may be either read off at each output simultaneously, or it can be shifted out and replaced.

In cases where the parallel outputs should not change during the serial loading process, it is desirable to use a latched or buffered output. In general, the practical application of the serial-in/parallel-out shift register is to convert data from serial format on a single wire to parallel format on multiple wires.

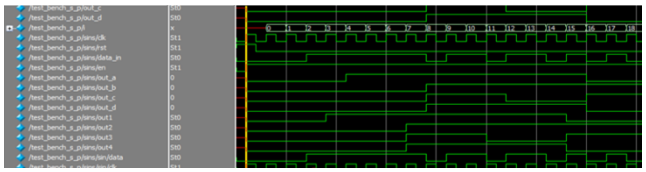

Fig 4. Serial to Parallel Converter

INTERLEAVER / DEINTERLEAVER

An interleaver, also known as a slicer, is an optical filter having at least one input and two complementary outputs. The data is interleaved by a block interleaver with a block size, which depends on the number of coded bits per allocated subchannels per OFDM symbol [9]. Interleaving is done to protect the data from burst errors during transmission. Conceptually, the in-coming bit stream is re-arranged so that adjacent bits are no more adjacent to each other. The data is broken into blocks and the bits within a block are rearranged. Talking in terms of OFDM, the bits within an OFDM symbol are rearranged in such a fashion so that adjacent bits are placed on non-adjacent subcarriers.

As far as De-Interleaving is concerned, it again rearranges the bits into original form during reception.

QPSK MODULATION

In the modulation mapper, the interleaved bits are converted to a sequence of complex valued symbols. WiMAX supports different modulation schemes such as QPSK, BPSK etc.The modulation constellation used in WiMAX is two types of phase shift keying (PSK) modulation (binary (BPSK) and quadrature (QPSK)) and two types of quadrature amplitude (QAM) modulation (16QAM and 64QAM). Her QPSK modulation was used.

A QPSK modulator can be implemented as follows [11]. A demultiplexer (or serial to parallel converter) is used to separate odd and even bits from the generated information bits. Each of the odd bits (quadrature arm) and even bits (in-phase arm) are converted to NRZ format in a parallel manner. The signal on the in-phase arm is multiplied by cosine component and the signal on the quadrature arm is multiplied by sine component. QPSK modulated signal is obtained by adding the signal from both in-phase and quadrature arm.

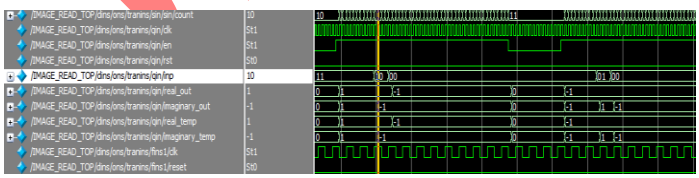

Fig 5. QPSK Modulation

INVERSE FAST FOURIER TRANSFORM (IFFT):

To convert mapped data, which is assigned to all allocated data subcarriers of the OFDM symbol, from frequency domain into time domain, the IFFT is used [8]. We can compute time duration of the IFFT time signal by multiply the number of FFT bins by the sample period. Zeros are added at the end and beginning of OFDM symbol. These zero carriers are used as guard band to prevent inter channel interference (ICI).

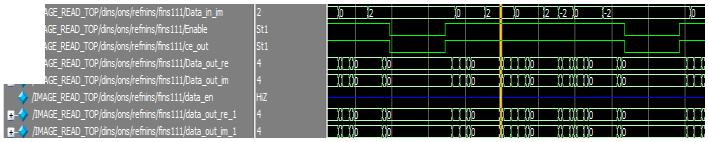

Fig 6. IFFT

CYCLIC PREFIX INSERTION (CP):

To avoid inter symbol interference (ISI) a cyclic prefix is inserted before each transmitted symbol [12]. That is achieved by copying the last part of an OFDM symbol to the beginning. WiMAX supports four different duration of cyclic prefix (i.e. assuming G is the ratio of guard time to OFDM symbol time, this ratio is equal to 1/32, 1/6, 1/8 and 1/4). In order to preserve the sub-carrier orthogonality and the independence of subsequent OFDM symbols, a cyclic guard interval is introduced. The guard period is specified in terms of the fraction of the number of samples that make up an OFDM symbol. The cyclic prefix contains a copy of the end of the forthcoming symbol. Addition of cyclic prefix results in circular convolution between the transmitted signal and the channel impulse response. Frequency domain equivalent of circular convolution is simply the multiplication of transmitted signal's frequency response and channel frequency response, therefore received signal is only a scaled version of transmitted signal (in frequency domain), hence distortions due to severe channel conditions are eliminated**.** Removal of cyclic prefix is then done at the receiver end and the cyclic prefix–free signal is passed through the various blocks of the receiver.

FAST FOURIER TRANSFORM (FFT)

To convert received data from time domain to frequency domain, the FFT is used [8]. Afterward, the zeros, which were added at the end and beginning of OFDM symbol (guard bands) at the transmitter are removed from the assigned places.

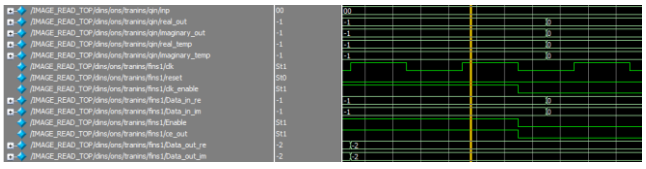

Fig 7. FFT

QPSK DE MODULATOR

The demodulator is used for de-mapping purpose. The demodulator assumes that the original message data stream was split into two streams, A and B, at the transmitter, with each converted to a PSK signal. The two PSK signals were then added, their carriers being in phase quadrature.

The demodulator consists of two PSK demodulators, whose outputs, after analog-to-digital (A/D) conversion, are combined in a parallel-to-serial converter [11]. This converter performs the recombination of the two channels to the original single serial stream. It can only do this if the carriers at the demodulator are synchronous, and correctly phased, with respect to those at the transmitter.

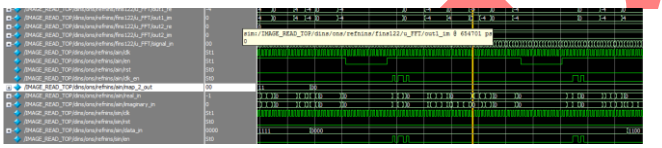

Fig 8. QPSK Demodulation

PARALLEL TO SERIAL CONVERTOR:

Here, the parallel data [9] that is obtained from the previous blocks is converted into serial data so that we can extract the compressed data. This parallel to serial convertor is an inverse of serial to parallel convertor. It also contains shift register.

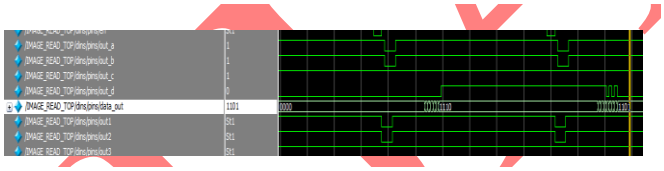

Fig 9. Parallel to Serial Converter

INVERSE DISCRETE FOURIER TRANSFORM (IDCT):

The inverse discrete cosine transform (IDCT) decodes an image into the spatial domain from a representation of the data better suited to compaction [12]. IDCT-based decoding forms the basis for current image and video decompression standards. The input to the IDCT comes after the de-spreading. An 8x8 block of input values range from -2048 to 2047 and output values in the range -256 to 255. This information is used to reconstruct the image.

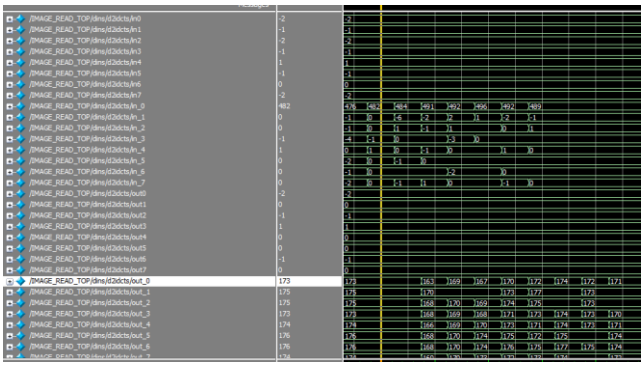

Fig 10. IDCT

The comparison between the input image and the reconstructed image is shown below.

Original Image

Output Image

There are some errors in the reconstructed image due to noise and burst errors. These errors can be removed using Forward Error Correction Mechanisms.

IV . ENERGY AWARE MAPPING TECHNIQUES.

Mapping Techniques consider energy as the main parameter. Thera are two types of mapping techniques namely task and core mapping.Quartur II tool was used for these techniques.

TASK MAPPING

Task mapping is based on a cost function that considers static, dynamic, and reconfiguration energy costs [1]. There is no corresponding available communication cost before initial mapping. The set of tasks with the minimum cost function is included and all the tasks are arranged based on utilization in descending order[1]. This heuristic starts

mapping tasks to the PUs with lower static power first. This increases the chance to pack more tasks into the instance with lower static power consumption, and contributes accordingly to the total energy saving.

The PU types are sorted in ascending order according to the static power consumption. Subsequently, the new energy cost is computed for each task on each PU instance . The new energy cost on each instance consists of static, dynamic, and reconfiguration energy. Thus, the task is mapped with the minimum total estimated cost. After mapping, the total utilization for each scenario *Sm* , and the mapping variable is updated. The algorithm of task mapping is shown below.

$\mathcal{T}_j \leftarrow \phi \; \forall \; P_j \in \mathcal{P}$
$Z_{m,j,k} = 0 \; \forall \; S_m \in \mathcal{S}, \; \hat{p}_{j,k} \in \mathcal{P}$
$U_{m,j,k} = 0 \; \forall \; S_m \in \mathcal{S}, \; \hat{p}_{j,k} \in \mathcal{P}$
for each $t_i \in \mathcal{T}$ **do**
  Determine P_j type which minimizes the expected energy consumption based on static, dynamic, and reconfiguration energy costs only such that $f_{i,j} = 1$ and $u_{i,j} \leq 1$.
  $P_j \leftarrow \arg \min_{P_j \in \mathcal{P}} \{u_{i,j}\zeta_i\sigma_j + \kappa_i^{av}\tau_{i,j}\delta_{i,j} + r_i\eta_{i,j}\tau_{r_{i,j}}\}$
  $\mathcal{T}_j \leftarrow \mathcal{T}_j \cup \{t_i\}$
end for
Sort PU types $P_j \in \mathcal{P}$ in ascending order according to static power consumption
for each $P_j \in \mathcal{P}$ **do**
  Sort all tasks in $\mathcal{T}_j$ in descending order according to the utilization $u_{i,j}$
  for each $t_i \in \mathcal{T}_j$ **do**
    for each $\hat{p}_{j',k'} \in \mathcal{P}$ **do**
      Let S_{t_i} be the set of scenarios which host task t_i
      $S\_cost_{i,j',k'} = \sum_{S_m \in S_{t_i}} \chi_m \tau_m Z_{m,j',k'}\sigma_{j'}$
      $D\_cost_{i,j',k'} = \kappa_i^{av}\tau_{i,j'}\delta_{i,j'}$
      $R\_cost_{i,j',k'} = r_i\eta_{i,j'}\tau_{r_{i,j'}}$
      $Cost_{i,j',k'} = S\_cost_{i,j',k'} + D\_cost_{i,j',k'} + R\_cost_{i,j',k'}$
    end for
    Assign t_i to $\hat{p}_{\check{j},\check{k}}$ such that:
    $\hat{p}_{\check{j},\check{k}} \leftarrow \arg \min_{\hat{p}_{j',k'}} \{Cost_{i,j',k'}\}$,
    $U_{m,\check{j},\check{k}} + u_{i,\check{j}} \leq 1 \; \forall \; S_m \in S_{t_i}$ and $f_{i,\check{j}} = 1$
    $U_{m,\check{j},\check{k}} = U_{m,\check{j},\check{k}} + u_{i,\check{j}} \; \forall \; S_m \in S_{t_i}$
    $Z_{m,\check{j},\check{k}} = 1 \; \forall \; S_m \in S_{t_i} \quad , \quad M_{i,\check{j},\check{k}} = 1$
  end for
end for

Fig 11. Task Mapping Algorithm

CORE MAPPING

Core Mapping is used to locate each utilized PU instance in a specific NoC position such that the communication energy is minimized [1]. This core mapping is based on the most recent task mapping. The set of utilized instances and The set of mapped and unmapped PU are taken into consideration. The core mapping is determined based on the average number of transactions between the different instances. The algorithm tends to map the instances with a larger number of transactions as close as possible [1]. This heuristic creates system level floorplanning to build a custom NoC architecture that is well suited for the target heterogeneous platform.

The algorithm for core mapping is given below.

$\mathcal{P}^o \leftarrow$ Set of occupied instances that host tasks
$P_p = \phi$; $P_u = \mathcal{P}^o$;
$R \leftarrow$ Set of feasible positions in X-Y plane
$Navg\_out_{j,k} \leftarrow$ Average 2-way comm. cost with each $\hat{p}_{j,k}$
$\hat{p}_{j_m,k_m} \leftarrow arg \max_{\hat{p}_{j,k} \in \mathcal{P}} \{Navg\_out_{j,k}\}$
$X^{min}_{j_m,k_m} = (0,0)$
$r \leftarrow$ Area bounded by $(X^{min}_{j_m,k_m}, Y^{min}_{j_m,k_m})$ and $(X^{max}_{j_m,k_m}, Y^{max}_{j_m,k_m})$
$P_p = P_p \bigcup p_{j_m,k_m}$; $P_u = P_u \backslash p_{j_m,k_m}$; $R = R \backslash r$;
while $P_u \neq \phi$ **do**
$\hat{p}_{j_m,k_m} \leftarrow arg \max_{P_j \in P_u} \{$2-way comm. cost with instances in $P_p\}$
$(X^{min}_{j_m,k_m}, Y^{min}_{j_m,k_m}) = (X,Y) \in R$ that minimizes the comm. energy cost with the between $\hat{p}_{j_m,k_m}$ and placed instances.
$r \leftarrow$ Area bounded by $(X^{min}_{j_m,k_m}, Y^{min}_{j_m,k_m})$ and $(X^{max}_{j_m,k_m}, Y^{max}_{j_m,k_m})$
$P_p = P_p \bigcup p_{j_m,k_m}$; $P_u = P_u \backslash p_{j_m,k_m}$; $R = R \backslash r$;
end while

Fig 12. Core Mapping Algorithm

The performance of the proposed heuristic for a set of realistic benchmarks that are widely used in Wi-Max Technology. The components that are used can be used for different applications also. These applications are profiled and divided into individual tasks as presented by the task graphs .

A total of 11 execution scenarios are assumed, where each one comprises of single or multiple applications with equal latency requirements and different throughputs. The different scenarios with their corresponding execution probabilities are taken into consideration. Here Nios II processor was considered as PU.

The area summary of the techniques are given below.

Flow Status	Successful - Sun Feb 01 13:53:53 2015
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	TOPMODULE
Family	Cyclone III
Met timing requirements	N/A
Total logic elements	11,091 / 24,624 (45 %)
Total combinational functions	10,385 / 24,624 (42 %)
Dedicated logic registers	4,258 / 24,624 (17 %)
Total registers	4259
Total pins	132 / 216 (61 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)
Device	EP3C25F324C6
Timing Models	Final

Fig 13. Task Mapping

Flow Status	Successful - Thu Oct 30 03:41:10 2014
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	TOPMODULE
Family	Cyclone III
Met timing requirements	N/A
Total logic elements	11,464 / 24,624 (47 %)
Total combinational functions	10,759 / 24,624 (44 %)
Dedicated logic registers	4,259 / 24,624 (17 %)
Total registers	4259
Total pins	132 / 216 (61 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)
Device	EP3C25F324C6
Timing Models	Final

Fig 14. Core Mapping

Thus, the PU types used for basic computations are sorted in ascending order according to the hierarchical structure of IP cores and initial core mapping for each utilized PU instance in a specific positions. All instances are mapped in different locations. The power dissipation from the core mapping technique is 104.15mW.

The comparison table for the mapping techniques is shown below.

TYPE	Area	Fmax
Core Mapping	11,464	88.91 MHz
TASK Mapping	11,091	85.6 MHz

Thus, it is seen that the task mapping technique uses less area than the core mapping technique.

V . CONCLUSION

Wi-MAX technology brought revolution in both fixed and mobile wireless communication. In present communication world, wireless communication does high speed data transmission. The Wi-Max Transceiver was designed using the discussed procedure as shown above. All the models used were conventional models. The image input was given through matlab and the output was taken from matlab using the .txt file. The output was fond to be in match with the original data. Then the area of transceiver was obtained using the energy mapping techniques. Finally the area and maximum frequency was compared. The implemented PHY layer model still needs some improvement in terms of rectifying errors. The channel estimator can be implemented to obtain a depiction of the channel state to combat the effects of the channel using an equalizer.

REFERENCES :-

1. Amr M. A. Hussien, Rahul Amin, Ahmed M. Eltawil, and Jim Martin," Energy Aware Mapping for Reconfigurable Wireless MPSoCs**,"** *IEEE Transactions On Very Large Scale Integration (VLSI) Systems***,** vol.7,no.4,pp. 1063-8210, 2014.
2. J. Huang, C. Buckl, A. Raabe, and A. Knoll, "REMiS: Run-time energy minimization scheme in a reconfigurable processor with dynamic powergated instruction set," in *Proc. IEEE/ACM Int. Conf. Comput. Aided Des. ICCAD Tech. Papers*, Nov. 2009, pp. 55–62.
3. J. Castrillon, R. Leupers, and G. Ascheid, "MAPS: Mapping concurrentdataflow applications to heterogeneous MPSoCs," *IEEE Trans. Ind.Informat.*, vol. 9, no. 1, pp. 527–545, Feb. 2013.
4. S. Murali, M. Coenen, A. Radulescu, K. Goossens, andG. De Micheli, "A methodology for mapping multiple use-cases onto networks on chips," in *Proc. Conf. Des., Autom. Test Eur.*, 2006,pp. 118–123.
5. W. Jang and D. Pan, "Dynamic power aware mapping of applications onto heterogeneous MPSoC platforms,"*IEEE Trans. Ind. Informat.*, vol. 6, no. 4, pp. 692–707,Nov. 2010.

6. Aseem Pandey, Shyam Ratan Agrawalla & Shrikant Manivannan, "VLSI Implementation of OFDM", *Wipro Technologies*, September 2002.
7. Ahmed R. S. Bahai and Burton R. Saltzberg, 'Multi Carrier Digital Communication". *Kluwer Academic Publishers*, 2002.
8. S. B. Weinstein and P. M. Ebert, "Data transmission by frequency division multiplexing using the discrete Fourier transform", *IEEE Trans. Communications*, COM-19(5): 628-634, Oct. 1971.
9. W.-H Tseng, et al. "Digital VLSI OFDM Transceiver Architecture for Wireless SoC Design", *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2005.
10. Jeffrey G. Andrews, Rias Muhammad, "Fundamentals of WIMAX". *Prentice Hal Communications Engineering*, 2006.
11. Shahid Abbas, *Student Member, IEEE*, Waqas Ali Khan, Talha Ali Khan and Saba Ahmed "OFDM Baseband Transmitter Implementation" Compliant IEEE Std 802.16d on FPGA2009
12. Nasreen Mev, Brig. R.M. Khaire, "Implementation of OFDM Transmitter and Receiver Using FPGA," I*nternational Journal of Soft Computing and Engineering (IJSCE)",* ISSN: 2231-2307, Volume-3, Issue-3, July 2013.