SPWM GENERATION USING CPLD BOARD

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ABSTRACT:

The Field Programmable Gate Array (FPGA) incorporates for the structure of control systems for inverters embraced in numerous industry applications, due to the two its high adaptability of utilization and its elite as for different kinds of computerized controllers. In this this paper a literature review is presented on the consonant substance of the voltages delivered by a three-stage, five level fell H-Bridge Multilevel inverter with a FPGA- based control board, pointing additionally to assess the performance benefits of the FPGA through the different research papers and studies through the primary basic adjustment methods and the correlation among reproduction and test results. Besides, the brief understanding of the inverter and an electric drive framework containing a staggered converter are revealed.

INTRODUCTION

Power electronics and electrical system is the technology that is associated with various types of sub technical aspects like control system, efficient conservation, storage system, distribution lines, Photovoltaic panels, and conditioning of electric power from its input in to desire controlled electrical form. Most of modern technology firmly depends upon power and energy technology. There are various research and technique that are available to improve the qualities of power, one of these techniques is the SPWM or sinusoidal pulse width modulation is widely used in power electronics to digitize the power so that a sequence of voltage pulse can be generated to control the ICBT power transistors. This review paper is about SPWM generation using CPLD board for 3 phase design of modular multilevel cascade (MMC) inverter system. In which reference is a sinusoidal wave at the frequency of the desired output signal and the carrier wave is a triangle or saw tooth wave which operates at a frequency significantly greater than the reference wave. During the modulation when the carrier signal exceeds the reference the output is at one state, and when the reference exceeds the carrier the output is at the opposite state then the output wave become Sinusoidal Pulse Width Modulation. The advantages of using SPWM in conversion of DC/AC helps in designing smaller filter size lower Electromagnetic Induction (EMI); lower Total Harmonic Distortion (THD). The control strategies for multilevel inverters is multilevel sinusoidal (PWM), the main purpose is to reducing Total Harmonic Distortion (THD) and provide switching function to H-bridges of multilevel inverters. This implementation is capable to support the high switching frequency requirements of modern power electronics DC to AC converters. The proposed SPWM unit has been implemented in a single chip in order to enable the reduction of the DC AC converter control unit complexity, cost and development time.

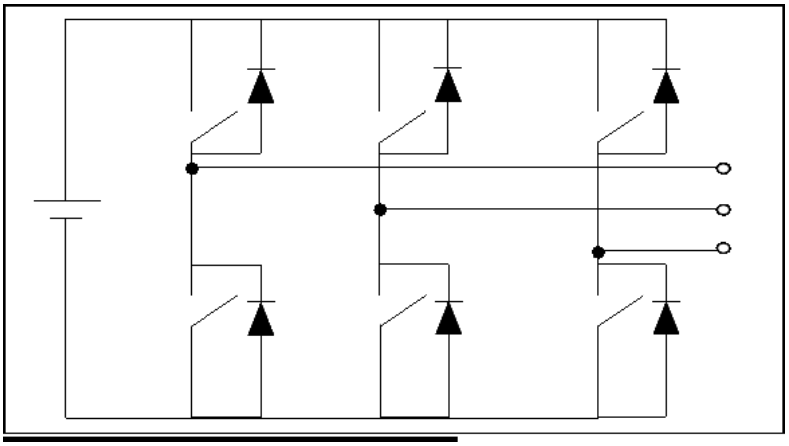
LITERATURE SURVEY

In the course of the most recent decades, the innovative advances of programming for the usage of computerized frameworks, which are by and large finished to the control of explicit applications, has altogether added to the improvement of the structure procedures of advanced controllers devoted for the electrical vitality transformation. Besides, the recently referenced element permits the acknowledgment of an arrangement of rationale activities created in equal, diminishing the figuring time what's more, prompting the accomplishment of superior control frameworks, which can be even analysed with identical controllers created by analogical segments.

A few papers in the writing have concentrated in the field of staggered converters constrained by FPGA, particularly for fast control frameworks For example, Islam et al, just as Zhou et al, proposed the displaying and test assessment of staggered inverters control, centring their enthusiasm towards the execution through FPGA and not on the consonant substance of the voltage waveform for the distinctive tweak methods. Comparative investigation and exploratory outcomes are given however for various instances of uses. Furthermore, Aime et al proposed the utilization of a FPGA for the Peak Current Control (PCC) in a staggered inverter: the principle assignments of the FPGA design, for example, incline age, dead time creation, exchanging orders age, and voltage guideline, are very much portrayed. Gateau et al feature the job of FPGA in the usage of an advanced sliding-mode spectator of the flying capacitors in stacked multicellular converters (SMCs). By and by, the expected advantages as far as THD improvement are not broadly demonstrated. In, Coppola et al. introduced a FPGA-based control technique for Cascade Half Bridge (CHB) inverters: in spite of a wide misuse of the FPGA assignments (e.g., Maximum Power Point Tracking, MPPT, and arranging calculation execution, dead time age, estimation stage) the FPGA framework isn't answerable for the PWM control, which is actualized by a DSP. Besides, the work depicted in considers just three balance methods, additionally eluding a few DSP drawbacks, for example, the expanded handling time or a decreased precision because of the restricted accessible assets. Notices of the adaptability of the FPGA framework as far as industry applications can be found in. Specifically recent papers address the control of secluded staggered converters, and others face the developing application on electrical portability from battery the board frameworks and footing. All proposed late papers report FPGA as the most fitting response for actualizing continuously the control strategies, because of its versatile equal handling equipment structure, which licenses executing assorted calculations with lessening the sequential and successive activities contrasted with customary CPU usage. In this unique situation, this paper expects to introduce a definite examination and test approval on the exhibitions as far as symphonies mutilation of the voltages delivered by a course h-connect staggered inverter, constrained by a FPGA and for a few regulation procedures.

SYSTEM DESIGN

DC-to-AC converters are known as inverters. The capacity of an inverter is to change a DC input voltage to a balanced AC output voltage of wanted size and recurrence. The yield voltage could be fixed or variable at fixed or variable frequency .The inverters can be worked by controlled turn-on and turn-off semiconductor gadgets, for example, Bipolar Junction Transistors (BJTs), power Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs), Insulated Gate Bipolar Transistors (IGBTs) and others. Inverters are widely used in modern applications (for example acceptance engine drive, induction heating, backup power flexibly, and uninterruptible force supplies). The VSI can be additionally isolated into a solitary stage inverter and a three-phase inverter. The three-stage VSIs are regularly utilized for high-power applications and broadly utilized for AC engine drives. A three-stage inverter is considered as three single-stage inverters and the yield of each single-stage inverter is moved by (120°), the chart of the force circuit of three-stage VSI is appeared in the figure below.



Three-phase bridge inverter circuit

The PWM techniques adopted for multilevel converters, namely MC PWM [35–40], are usually the same as those applied for traditional converters. The common techniques for Multilevel Power Inverter (MPI) use several triangular carrier signals and one modulating signal per phase. By taking into account the CHBMI topology, the command signals delivered to the components of the same leg of the bridge are obtained through the comparison between each carrier signal and the modulating signal. For a MPI with a number of levels equal to nL, the number of carrier signals Nc is given by the following equation:

$$Nc = nL - 1$$

The modulation index m can be expressed as function of

$$nL: m = AM\ AC(nL - 1)$$

where AM is the amplitude of the modulating signal, whereas AC is the amplitude of the carrier

signal. Moreover, the frequency modulation index, namely mf , is given by the ratio between the frequency of the carrier signal fC and the frequency of the output fundamental signal f 1:

$$mf = fC\ f1 \quad (5)$$

In the literature, several MC PWM modulation techniques for multilevel inverters are provided. In particular, depending on the phase shift among the carrier signals, the following dispositions can be obtained

- Phase Disposition PWM–PD PWM (Figure 2a);
- Phase Opposition Disposition PWM–POD PWM (Figure 2b);
- Alternative Phase Opposition Disposition PWM APOD PWM (Figure 2c);
- Phase Shifted - PS PWM (Figure 2d)

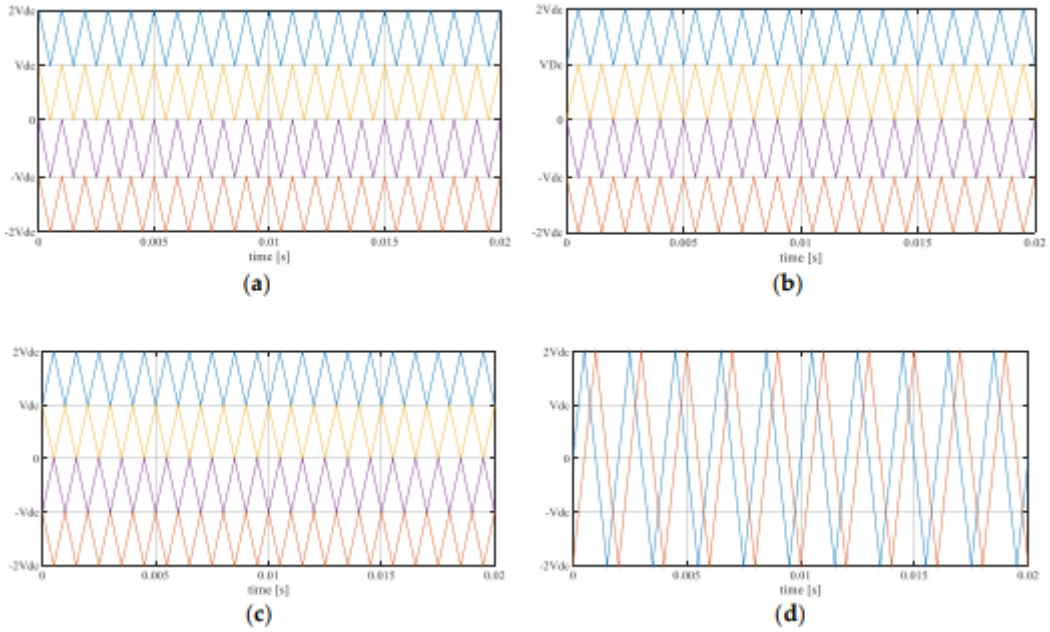
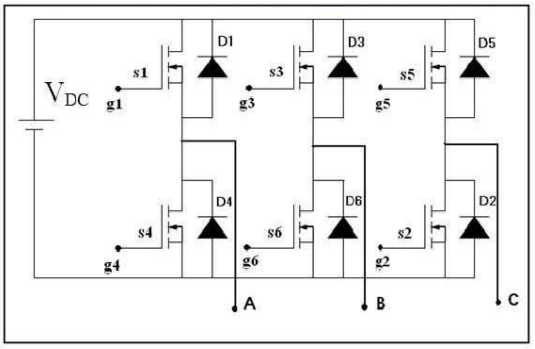


Figure 2. Multicarrier modulation techniques for five-level inverter. (a) Sinusoidal Phase Disposition (SPD). (b) Sinusoidal Phase Opposition Disposition (SPOD). (c) Sinusoidal Alternative Phase Opposition Disposition (APOD). (d) Sinusoidal Phase-Shifted (SPS).

IMPLEMENTATION SYSTEM

The PWM signals from the matching circuits are connected to switches gate pin in the three-phase bridge inverter circuit. The basic three-phase bridge inverter circuit is shown in Fig below. The power switch type chosen for the voltage source bridge inverter is the (IRFP450). The switch is an N-Channel power MOSFET (Metal Oxide Semiconductor Field-Effect Transistor). It is a rugged

device, capable of withstanding voltages up to 500V and currents up to 14A. In addition, it has a built-in fast recovery diode, useful when inductive loads and stray inductances are present in the circuit.



Three-phase bridge inverter circuit

CONCLUSION

In this review paper the generation of PWM gating signals for the three-phase VSI switches based on FPGA was successfully realized. Using FPGA to generate PWM provides flexibility to modify the designed circuit without altering the hardware part, easy and fast circuit modification, comparatively low cost for a complex circuitry and rapid prototyping. The control algorithm of the three-phase VSI was constructed in the FPGA chip, also the hardware equipment needed for this driver were constructed using a three-phase bridge inverter and gate driving circuit.

FUTURE SCOPE

There are a few thoughts for future work and proposals to improve this exploration, the accompanying focuses show these ideas:

1. Try to Apply a closed loop V/F control for IM drive.

2. Utilizing SVM procedure dependent on FPGA to produce PWM rather of SPWM, in light of the fact that the SVM offers numerous points of interest contrasted with the SPWM.

3. Applying vector control procedure where both the greatness and phase of the control factors are controlled.4.

4. Applying on-line dead-time remuneration procedure based on FPGA

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